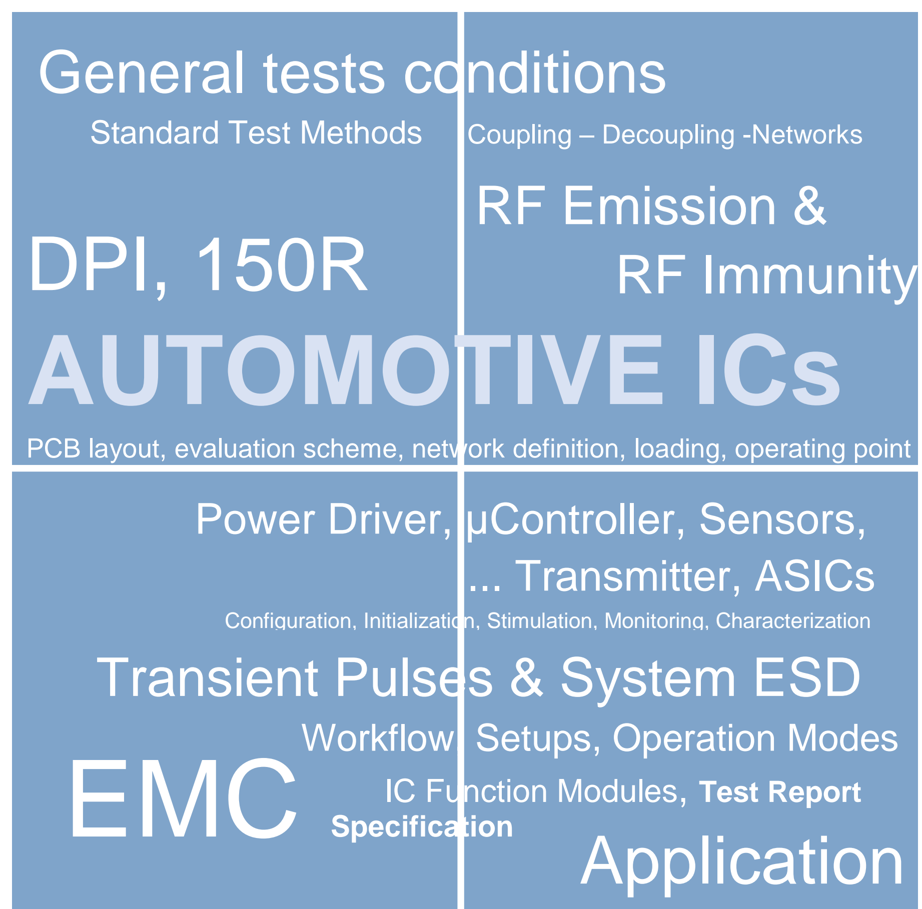
ZVEI: Die Elektroindustrie

Generic IC EMC Test Specification

Version 2.1



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The document can be found at: http://www.zvei.org/generic-ic-emc-test-specification

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1 Scope

This document defines common tests characterising the EMC behaviour of integrated circuits (ICs) in terms of RF emission and RF immunity in the frequency range from 150 kHz up to 3 GHz as well as pulse immunity and system level ESD*), based on international standards for integrated circuits and related standards for IC applications. It contains all information to evaluate any kind of ICs in the same way. In this document general information and definitions of IC types, pin types, test and measurement networks, pin selection, operation modes and limit classes are given. This allows the user to create an EMC specification for a dedicated IC as well as to provide comparable results for comparable ICs.

*) Note: Unpowered system level ESD test covered, powered system level ESD test under consideration

2 Normative Reference

2.1 International standards

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

RF Emission:

[1] IEC 61967-1 Ed. 1: 2002, Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 1: General conditions and definitions

[2] IEC 61967-2 Ed. 1: 2005, Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 2: Measurement of radiated emissions – TEM cell and wideband TEM cell method

[3] IEC 61967-4 Ed. 1: 2006, Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method

[4] CISPR 25 3rd Ed. 2008-03: Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers

[5] IEC 61967-8 Ed.1: 2011 Integrated Circuits – Measurement of Electromagnetic Emissions Part 8: Measurement of radiated emissions – IC stripline method

RF Immunity:

[6] IEC 62132-1 Ed. 1: 2006, Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 1: General and definitions

[7] IEC 62132-2 Ed. 1: 2010, Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 2: Measurement of radiated immunity – TEM Cell and Wide Band TEM Cell Method

[8] IEC 62132-4 Ed. 1: 2006, Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF Power Injection Method

[9] IEC 62132-8 Ed. 1:2012, Integrated circuits – Measurement of electromagnetic immunity – Part 8: Measurement of radiated immunity – IC stripline method

Transient voltages:

[10] IEC 62215-3 Ed.1: Integrated circuits – Measurement of impulse immunity – Part 3: Non-synchronous transient injection method

[11] ISO 7637-2 3rd Ed. 2011, Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only

[12] ISO 7637-3 2nd Ed. 2007-07-01: Road vehicles – Electrical disturbances from conduction and coupling – Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines

Electrostatic discharge:

[13] IEC61000-4-2 2nd Ed. 2008, Electromagnetic compatibility (EMC) – Part 4: Testing and measuring techniques – Section 2: Electrostatic discharge immunity test – Basic EMC publication

[14] ISO 10605 2nd Ed. 2008-07-15: Road vehicles – Test methods for electrical disturbances from electrostatic discharge

[15] EIA JEP155A: 01/2012 Recommended ESD target levels for HBM/MM qualification

[16] EIA JEP157: 10/2009 Recommended ESD-CDM target levels

[17] ANSI/ESDA/JEDEC JS-001-2011, Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) – Component Level

[18] JESD22-C101E 12/2009: Field-Induced Charged-Device Model Test Method For Electrostatic Discharge Withstand Thresholds of Microelectronic Components:

2.2 Other relevant documents

[19] IEC 62228 TS Ed. 1: 2007: Integrated circuits – EMC evaluation of CAN transceivers

[20] Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications, Version 1.3, 2012

[21] ISO11452-1 Road vehicles — Component test methods for electrical disturbances from narrowband radiated electromagnetic energy — Part 1: General principles and terminology

[22] Hall/Hall/McCall, High Speed Digital System Design, issue 2000, ISBN 0-471-36090-2

2.3 Internet references

[IEV] http://www.electropedia.org/iev/iev.nsf/Welcome?OpenForm&Seq=1

3 Definitions and Abbreviations

3.1 Definitions

- **analog**
  Pertaining to the representation of information by means of a physical quantity which may at any instant within a continuous time interval assume any value within a continuous interval of values. Note: - The quantity considered may, for example, follow continuously the values of another physical quantity representing information.
  [IEV 101-12-05]

- **core**
  An → *IC function module* without any connection to outside of the IC via pins. (*Note:* The supply is connected via the *IC function module supply* to pins, signals to pins are connected via *IC function module driver*)

- **digital**
  Pertaining to the representation of information by distinct states or discrete values.
  [IEV 101-12-07]

- **EMC pin type**

  global pin

  A 'global' pin carries a signal or power, which enters or leaves the application board without any active component in between.

  local pin

  A 'local' pin carries a signal or power, which does not leave the application board. It remains on the application PCB as a signal between two components.

- **fixed function unit (FFU)**
  Functional core sub-unit of the → *IC function module 'Core'*, designed to perform one fixed function without instruction decoding and executing capability.

- **function**
  A set of relations which determines the value of the output variable from a given state of a system and the simultaneous value(s) of the input variable(s)
  [IEV 351-29-08, "Output function"]

- **IC type**
  IC with a characteristic set of functions built in. These functions are realized with → *IC function modules*.

- **IC function module**
  An *IC function module* is a device functional part of an IC with at least one function and its supply connection, if needed. (see also Figure 1)

  Passive IC function module: No supply system for function

  Active IC function module: A dedicated supply connection needed for function.

  Note: The supply connection is handled as a separate input/output pair as it has a dedicated EMC behavior.

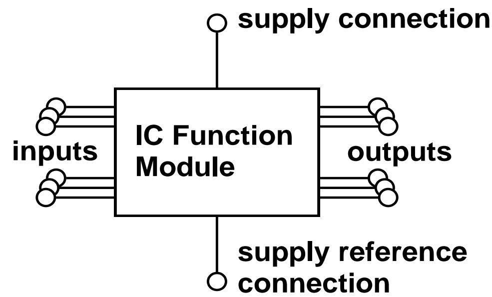


Figure 1: Common definition of an IC function module

- **integrated circuit (IC)**
  An integrated circuit (IC) is a set of implemented → *IC function modules* in one die or package.

- **mandatory components**
  Mandatory components are components needed for proper function of IC function modules as specified by the IC manufacturer (e.g. application note).

- **pin**
  Interface between an IC and its circuit environment.

- **port**
  An → *IC function module* containing minimum one d*river* and/or minimum one *input* each connected to a signal pin.

  active port
  An active port is initialized to a defined configuration or connected to *a →fixed-function module* unit and is in operating mode during EMC measurements.

  inactive port
  An inactive port is initialized to a defined configuration or connected to *a →fixed-function module* unit and remains in a defined static mode.

- **power net**
  Main Power Supply of an application system.

- **printed circuit board (PCB):**
  A piece of isolating material with fixed metal traces to connect electronic components.

- **sub supply net**
  Supply Net derived from Power Net.

- **supply pin pairs**
  Supply pin pairs are all supply voltage pins of the same supply voltage system with their related ground pin(s) of an IC supply module.

- **system level**

  Application-like test conditions (e.g. taken from electronic control unit requirements) directly applied on IC pins with or without external components

3.2 Abbreviations

AM	Amplitude Modulation
BAN	Broadband Artificial Network
BW	Bandwidth
CAN	Controller Area Network
CDM	Charged Device Model
CW	Continuous Wave
DPI	Direct Power Injection
E-Field	Electric Field
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FFU	Fixed Function Unit
GTEM-Cell	Gigahertz Transversal Electromagnetic Wave Cell
IC	Integrated Circuit
I/O	Input / Output
H-Field	Magnetic Field
HBM	Human Body Model
HSD	High Side Driver
LIN	Local Interconnect Network
LNA	Low Noise Amplifier
LSD	Low Side Driver
LVDS	Low Voltage Differential Signalling
LVR	Linear Voltage Regulator
PCB	Printed Circuit Board
PM	Pulse Modulation
RBW	Resolution Bandwidth
RF	Radio Frequency
SMPS	Switched Mode Power Supply
TEM-Cell	Transverse Electromagnetic Cell

4 General

4.1 Objective

The objective and benefit of the document is

- to obtain relevant quantitative IC EMC measurement results
- to reduce the number of IC EMC test methods to a necessary minimum
- to strengthen the acceptance of IC EMC test results
- to minimize EMC test effort to get comparable results for IC suppliers and users
- to release ICs based on IC level EMC results

4.2 Workflow for selection and test

The following recommended workflow shows in sequential order the steps required to generate a dedicated IC EMC specification and to perform the EMC measurements. A template of the IC EMC specification is provided in Chapter 12.

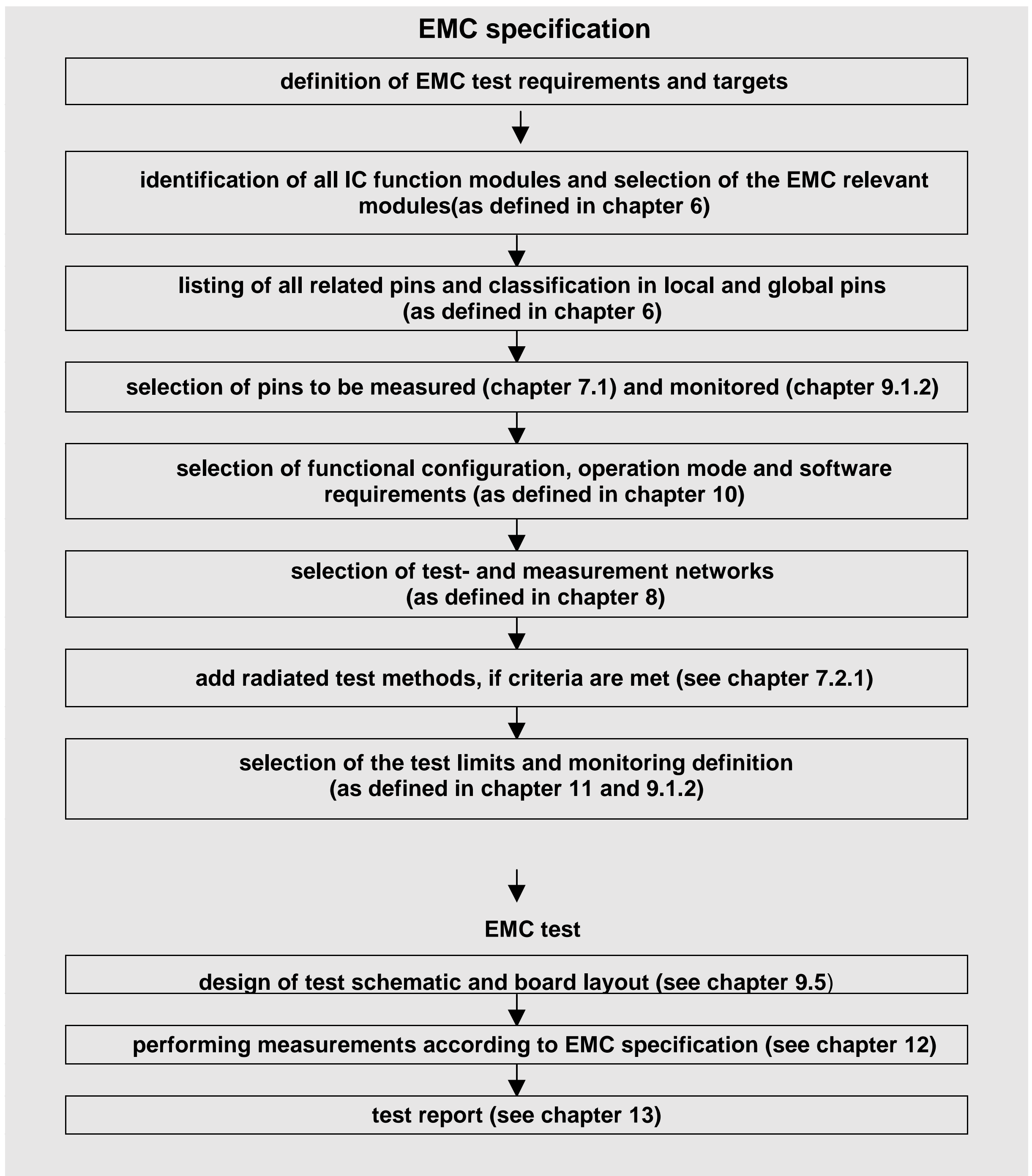


Table 1: Workflow to perform IC EMC measurements

5 Test definitions

5.1 Test methods

5.1.1 Conducted RF test methods

The conducted RF tests have to be performed for all ICs.

test type	coupling method	method name	reference
conducted emission	direct coupling via 150 Ω / 1 Ω network	150 Ω / 1 Ω method	IEC61967-4
conducted immunity	direct RF-power injection via DC block capacitor	direct power injection (DPI)	IEC62132-4

Table 2: Conducted test methods

5.1.2 Radiated RF test methods

The radiated RF tests have to be performed only for dedicated ICs, see chapter 7.2.1.

test type	coupling method	method name	reference
radiated emission	E- and H-field radiation of entire IC	(G)TEM-cell method	IEC61967-2
		IC stripline	IEC61967-8
radiated immunity	E- and H-field radiation on entire IC	(G)TEM-cell method	IEC62132-2
		IC stripline	IEC62132-8

Table 3: Radiated test methods

5.1.3 Transient pulse test methods

The transient pulse tests have to be performed for all ICs if transient exposure is expected, see chapter 7.1.5.

test type	coupling method	method name	reference
transient immunity	direct transient coupling	non-synchronous transient injection	IEC62215-3
	capacitive transient coupling		

Table 4: Transient test methods

5.1.4 ESD Test methods

Unpowered system level ESD tests have to be performed only for dedicated IC pins, see chapter 7.1.7.

test type	coupling Method	model	reference
IC level ESD	contact discharge	HBM-IC	ANSI/ESDA/JEDEC JS-001-2011
IC level ESD	contact discharge	CDM	JESD22-C101E
system level ESD	contact discharge	HBM-System	ISO10605 2nd Ed

Table 5: ESD Test methods

5.2 Test parameters

5.2.1 General test conditions

Environment: Temperature 23°C +/-5°C
Supply: Nominal voltage +/- 5%

5.2.2 RF Emission: Bandwidths and frequency step sizes

For all measurements the noise floor must be minimum 6 dB below the limit.

<table>
<tr><th colspan="5" rowspan="2">method</th><th rowspan="2">frequency range</th><th colspan="2">receiver****)</th></tr>
<tr><th>RBW</th><th>step size</th></tr>
<tr><td rowspan="2">1 Ω</td><td rowspan="3">150 Ω</td><td rowspan="3">µTEM</td><td rowspan="4">GTEM ***)</td><td rowspan="4">IC stripline</td><td>150 kHz to 30 MHz</td><td>9 kHz / 10 kHz</td><td>4,5 / 5 kHz</td></tr>
<tr><td>30 MHz to 200 MHz</td><td rowspan="3">100 kHz / 120 kHz**)</td><td rowspan="3">50 / 60 kHz</td></tr>
<tr><td>*)</td><td>200 MHz to 1000 MHz</td></tr>
<tr><td></td><td></td><td></td><td>1000 MHz to 3000 MHz</td></tr>
</table>

Table 6: General test parameters: Emission with RF receiver

*) **Note:** Upper frequency range of 1 Ω method is critical to handle, see layout recommendations
) **Note: Instead of 120 kHz / 100 kHz a bandwidth of 10 kHz / 9 kHz (with appropriate step size) can be used to reduce the noise level in case of no difference of the disturbances.
***) **Note:** The GTEM cell can be used above 3 GHz for homologation of transmitter applications according to ETSI and FCC specifications
****) **Note:** Time domain FFT analyzers can also be used if the results are identical

<table>
<tr><th colspan="5" rowspan="2">method</th><th rowspan="2">frequency range</th><th colspan="2">analyzer</th></tr>
<tr><th>RBW</th><th>sweep time**)</th></tr>
<tr><td rowspan="2">1 Ω</td><td rowspan="3">150 Ω</td><td rowspan="3">µTEM</td><td rowspan="4">GTEM ****)</td><td rowspan="4">IC stripline</td><td>150 kHz to 30 MHz</td><td>9 kHz / 10 kHz</td><td rowspan="4">$t_s = \frac{NP \cdot LT \cdot FR}{RBW}$</td></tr>
<tr><td>30 MHz to 200 MHz</td><td rowspan="3">100 kHz / 120 kHz***)</td></tr>
<tr><td>*)</td><td>200 MHz to 1000 MHz</td></tr>
<tr><td></td><td></td><td></td><td>1000 MHz to 3000 MHz</td></tr>
</table>

Table 7: General test parameters: Emission with RF analyser

*) **Note:** Upper frequency range of 1 Ω method is critical to handle, see layout recommendations
) **Note: NP = Number of Points; LT = Loop time or minimum period; FT = Frequency range
***) **Note:** Instead of 120 kHz / 100 kHz a bandwidth of 10 kHz / 9 kHz (with appropriate step size) can be used to reduce the noise level in case of no difference of the disturbances.
****) **Note:** The GTEM cell can be used above 3 GHz for homologation of transmitter applications according to ETSI and FCC specifications

Detector type: Peak detector

Measurement time: The emission measurement time at one frequency shall be minimal the period or test software loop time (LT).

5.2.3 Immunity against RF disturbances

Frequency step sizes

Frequency step sizes related to frequency ranges are shown in Table 8. Critical frequencies such as clock frequencies, system frequencies of RF devices etc. should be tested using smaller frequency steps agreed by the users of this procedure. Deviations have to be stated in the test report.

<table>
<tr><th colspan="4" rowspan="2">method</th><th colspan="3" rowspan="2">frequency range</th><th>step size</th></tr>
<tr><th>linear</th></tr>
<tr><td rowspan="6">DPI</td><td rowspan="6">µTEM</td><td rowspan="7">GTEM *)</td><td rowspan="7">IC stripline</td><td>150 kHz</td><td>to</td><td>1 MHz</td><td>100 kHz</td></tr>
<tr><td>1 MHz</td><td>to</td><td>10 MHz</td><td>0,5 MHz</td></tr>
<tr><td>10 MHz</td><td>to</td><td>100 MHz</td><td>1 MHz</td></tr>
<tr><td>100 MHz</td><td>to</td><td>200 MHz</td><td>2 MHz</td></tr>
<tr><td>200 MHz</td><td>to</td><td>400 MHz</td><td>4 MHz</td></tr>
<tr><td>400 MHz</td><td>to</td><td>1000 MHz</td><td>10 MHz</td></tr>
<tr><td></td><td></td><td>1000 MHz</td><td>to</td><td>3000 MHz</td><td>20 MHz</td></tr>
</table>

Table 8: General test parameters for immunity

*) **Note:** The GTEM cell can be used above 3 GHz for homologation of transmitter applications according to ETSI standards and FCC rules

Dwell time

at each frequency should be set according to the loop time but at least 1000 ms.

DPI immunity result diagram

shows the maximum applied RF forward power without any monitored failures.

(G)TEM or IC stripline immunity result diagram

shows the maximum applied field strength calculated from the forward power (substitution method) without any monitored failures.

Modulation definition

<table>
<tr><th rowspan="2">Modulation</th><th colspan="2">frequency range</th></tr>
<tr><td>150 kHz – 800 MHz</td><td>800 MHz – 3000 MHz</td></tr>
<tr><td>CW</td><td colspan="2">A</td></tr>
<tr><td>AM</td><td>B</td><td></td></tr>
<tr><td>PM</td><td></td><td>B</td></tr>
</table>

Table 9: Modulation frequency ranges

A: The continuous wave (CW) test is mandatory.

B: A modulation test (AM, PM) is optional.

Amplitude modulation:

Parameters: 1 kHz, 80%, according to ISO 11452-1 automotive specifications: reduced carrier for same peak CW and AM (see Annex E). The frequency range is 150 kHz up to 800 MHz.

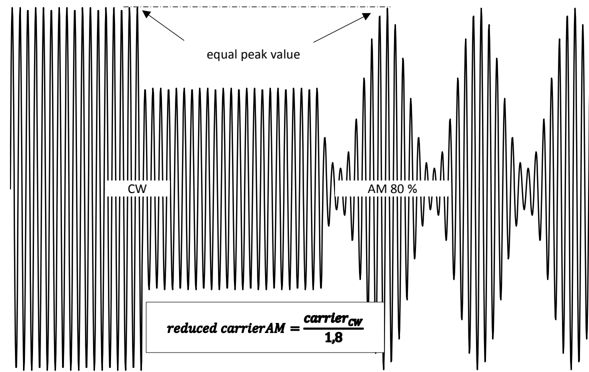


Figure 2: General test parameters: Immunity, definition of AM modulation carrier

Pulse modulation (PM):

Parameters (modulation similar to GSM standard): t_{on} = 577 µs and period T = 4600 µs. The frequency range is 800 MHz up to 3000 MHz.

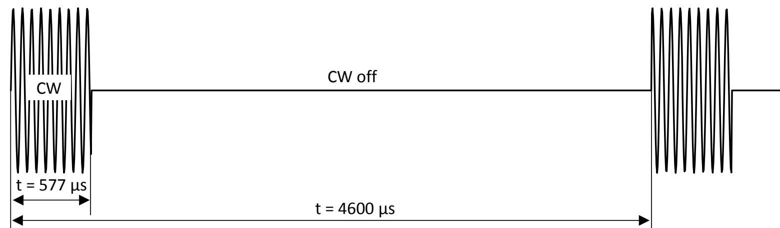


Figure 3: General test parameters: Immunity, definition of PM modulation carrier

5.2.4 Immunity against transient pulses

pulse	main waveform parameters				number of pulses / test duration	remarks
	R_i	t_d	t_r	t1		
1	10 Ω 50 Ω*)	2 ms 1 ms*)	1 µs 3 µs*)	0,5 s	500 pulses	supply cut off time t_2 is specified with 200 ms
2a	2 Ω 10 Ω**)	50 µs	1 µs	0,2 s	500 pulses	
3a	50 Ω	150 ns	5 ns	100 µs	10 min	
3b	50 Ω	150 ns	5 ns	100 µs	10 min	
user specific	other pulse definitions according to IEC 62215-3					

Table 10: Pulse parameter definitions

*) **Note:** values for 24V applications

) **Note: on special request (e.g. German OEM)

5.2.5 Immunity against ESD

pins	model	component values		standard	ESD level	remark
		C	R			
all pins	HBM	100 pF	1500 Ω	ANSI/ESDA/JEDEC JS-001-2011	≤ 1 kV*) or customer specific	IC level ESD test (for information, not part of this specification)
all pins	CDM	IC specific		JESD22-C101E	≤ 250 V*) or customer specific	
global pins	HBM	150 pF	330 Ω	ISO10605 2nd Ed.	2 kV 4 kV 6 kV or customer specific	system level ESD test

Table 11: ESD test definition

*) **Note:** Recommended ESD levels HBM acc. to JEDEC Publication 155A (JEP 155A) and CDM JEDEC Publication 157 (JEP 157)

To derive a statistical result at least 3 samples have to be tested. If a higher sample number is preferred for e.g. test automation a certain number of samples for each test level can be used as well.

#	Step	implementation	remark
1	pre-measurement	e.g. DC sweep over DC operating conditions, full parameter test, …	"0-point" measurement with defined max. current condition e.g.10 µA
2	pre-charge prevention	R_d ≥ 220 kΩ at all pins under test to GND implemented on PCB	ensure no pre-charging of the pin under test prior testing
3	start level	+/- 1 kV	default, if not otherwise specified
4	number of pulses	3 pulses of each polarity with discharge after each single pulse	for analyses 3 pulses of one polarity recommended
5	discharge of pin under test	R_d ≥ 220 kΩ at all pins under test to GND implemented on PCB	min. 1 sec. discharge time between pulses
6	post-measurement	e.g. DC sweep over DC operating conditions, full parameter test, …	once for each test level
7	voltage step	1 kV	default, if not otherwise specified
8	Loop	repetition of steps 2 to 7 till max. test voltage level or failure criteria is reached	

Table 12: Test procedure system level ESD

6 IC function modules

6.1 General

To define the relevant IC function modules influencing the EMC behaviour of an IC significantly all integrated functions have to be classified according to the following definitions.

6.2 Port module

A port consists of minimum one *port module* as defined below.

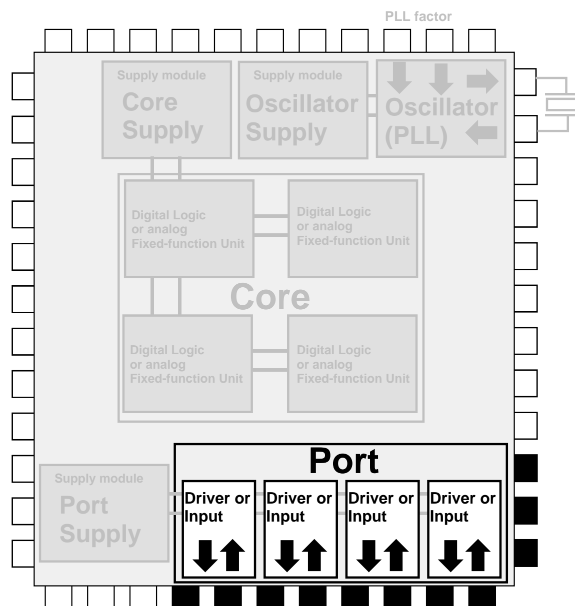


Figure 4: Port module

Port modules are:

a) **Line driver**

drives a signal leaving the application board (global pin).
Examples: ISO9141 outputs, LIN outputs, RF outputs

b) **Line receiver**

receives a signal from outside of the application board (global pin).
Examples: ISO9141 inputs, LIN inputs, RF inputs

c) **Symmetrical line driver**

drives a differential signal leaving the application board with two phase-correlated outputs (global pin).
Examples: CAN outputs, LVDS outputs

d) **Symmetrical line receiver**

receives a differential signal from outside of the application board with two phase-correlated inputs (global pin).
Examples: CAN inputs, LVDS inputs

e) **Regional driver**

drives a signal not leaving the application board (local pin).
Examples: serial data outputs, operational amplifier outputs, RF outputs

f) Regional input

receives a signal from the application board (local pin).
Examples: serial data inputs, Input stages of operational amplifiers, analog-digital-Converter (ADC) inputs, RF inputs

g) High side driver

drives power into loads. The current flows out of the driver (local or global pin).
Examples: High side switch, Switched mode power supply current output (buck converter)

h) Low side driver

drives power into loads. The current flows into the driver (local or global pin).
Examples: Low side switch, Switched mode power supply current input (boost converter)

i) RF antenna driver

drives a radio frequency signal into an antenna matching circuitry.
Example: RF amplifier

j) RF antenna receiver

receives an RF signal via an antenna matching circuitry.
Example: Low noise amplifier (LNA)

6.3 Supply module

A supply module distributes supply current to at least one IC function module (local or global pin).

It is an IC function module with at least one current input pin of the same supply system and minimum one current output. It may contain active elements like voltage stabilization and/or passive elements like internal charge buffering, current limiting elements etc.

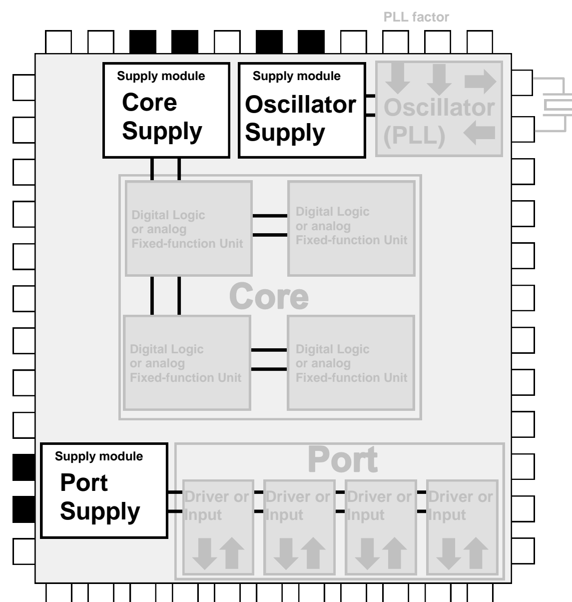


Figure 5: Supply module

6.4 Core module

A core module is an IC function module without any connection to outside of the IC via pins. The core is supplied via the IC function module supply. It contains a set of minimum one core module described below.

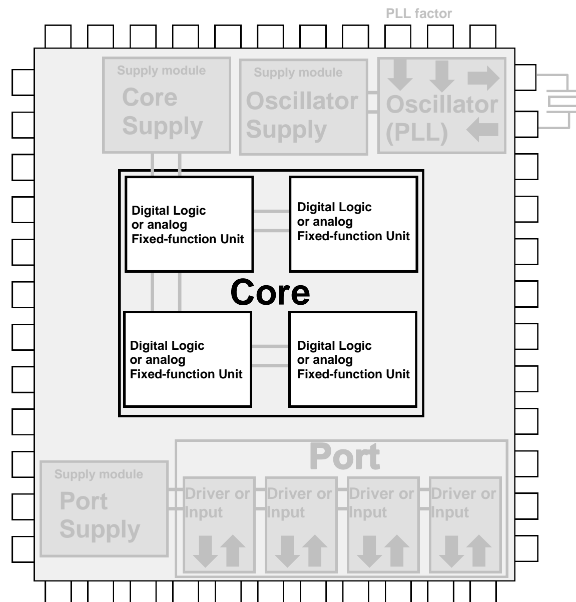


Figure 6: Core module

Core modules are:

Central processing unit (CPU)

A CPU decodes and executes instructions, can make decisions and jump to a new set of instructions based on those decisions.
Sub-units within the CPU decode and execute instructions (Sub-Unit CU (Control Unit)) and perform arithmetic and logical operations (Sub-Unit ALU (Arithmetic/Logic Unit)), making use of small number-holding areas called registers.

Digital logic fixed-function unit

Functional core sub-unit, designed to perform one fixed core digital logic function without instruction decode and execute capability.
Examples: Clock distribution, Memory logic and arrays, Registers, Timer, Watchdog Timer, State Machines, Programmable Logic Arrays (PLA).

Analog fixed-function unit

Functional core analog sub-unit, clocked or unclocked, designed to perform one fixed core analog function without instruction decode and execute capability.
Examples: Analog-to-digital-converter (ADC), Digital-to-analog-converter (DAC), Sample-and-hold-circuits, Switched capacitor filter, Charge Coupled Devices (CCDs).

Dedicated analog fixed function unit: Sensor element

A sensor element is a converter of an environmental value into an electrical value and therefore a FFU.

Examples: Hall sensor element for magnetic field sensing, E-field sensing, Acceleration sensing. It can be combined with a precision amplifier (FFU), a supply module and a line driver to realize an IC type "sensor".

6.5 Oscillator module

A oscillator module generates a periodic signal internally as a charge pump or clock generator by using a combination of a fixed function module of the core with regional drivers and regional inputs. Due to the EMC behaviour it is dedicated to be defined as a separate IC function module.

A fixed-frequency-oscillator may be part of a phase locked loop (PLL) circuit with voltage controlled oscillator (VCO), low pass filter, frequency divider and phase detection. All pins related to these circuits (for example divider, digital logic input pins) are part of this IC function module.

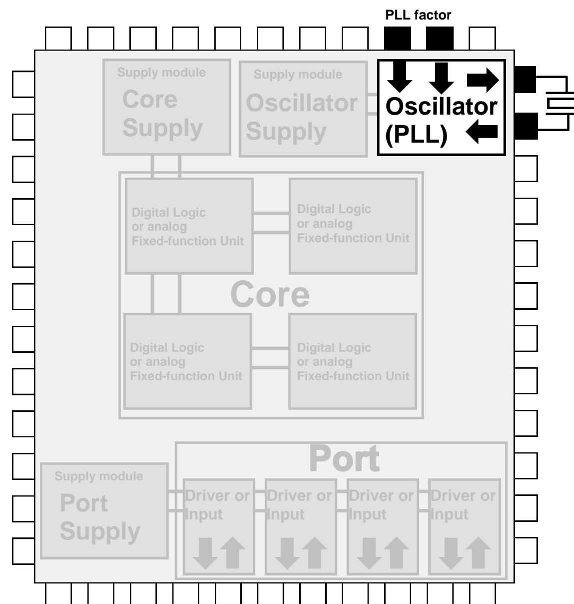


Figure 7: Oscillator module

6.6 Splitting ICs into IC function modules

6.6.1 Matrix for splitting ICs

IC type examples \ functional module		connection external circuit via pin											no pin			local external circuits
		driver (outputs)					inputs					supplies	core			core/ inputs
		line driver	symmetrical line driver	regional driver	high side driver	low side driver	RF antenna driver	RF antenna receiver	line receiver	symmetrical line receiver	regional input	all IC function module supplies	digital fixed function unit	analog fixed function unit	central processing unit (CPU)	oscillator
digital ICs	microcontrollers			•							•	•	•	•	•	•
digital ICs	RAM, ROM, bus drivers			•							•	•	•			
digital ICs	logic gate ICs			•							•	•	•			
analog ICs	operational amplifier	(•)	(•)	•							•	•		•		
analog ICs	VCOs			•							•	•		•		•
analog ICs	sensor circuit	•	(•)	(•)								•		•		
analog ICs	RF transmitter, RF power amplifier						•				•	•		•		•
analog ICs	RF receiver, low noise amplifier			•				•				•		•		•
power driver	high side driver (HSD)			(•)							•	•	•	(•)		(•)
power driver	low side driver (LSD)			(•)	•	•					•	•	•	(•)		
power driver	bridge			(•)	•	•					•	•	•	(•)		(•)
interface driver	symmetrical communication (e.g. CAN, LVDS)		•	•						•	•	•	•	(•)		(•)
interface driver	asymmetrical communication (e.g. LIN, Single Wire CAN)	•		•					•		•	•	•	(•)		(•)
linear voltage regulator (LVR)				(•)	•				•		(•)	•	(•)	(•)		
switched mode power supply (SMPS)				(•)	•	(•)			•		(•)	•	(•)	(•)		(•)
ASICs		any combination														

• = typical configuration

(•) = additional or alternative configuration

Table 13: Matrix showing which typical IC function module is integrated in several well known ICs

6.6.2 Example of an IC built up with IC function modules

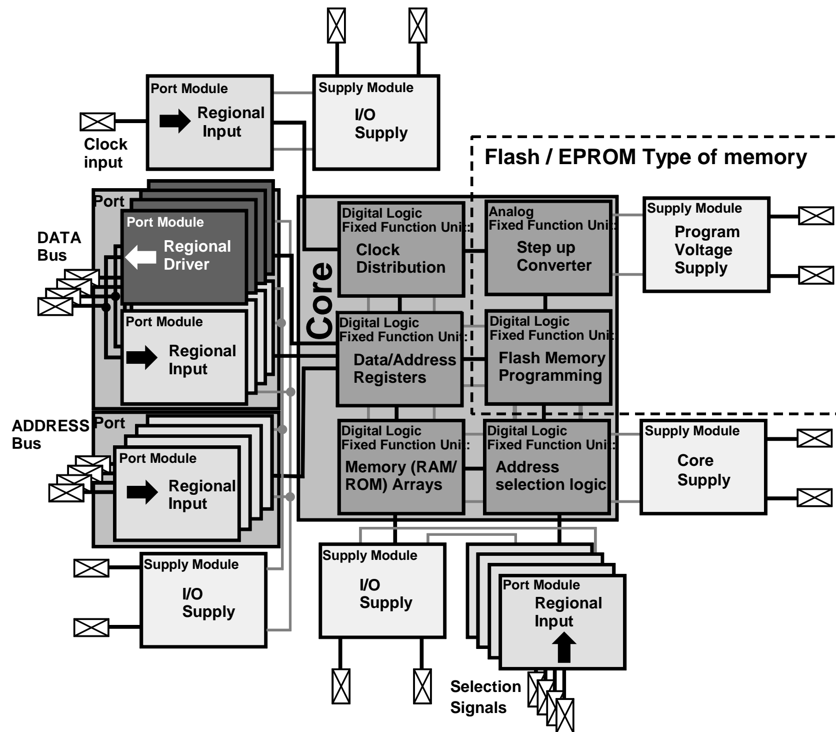


Figure 8: Example of a Memory IC built up with the IC function modules

7 Selection guide for test configuration

7.1 Conducted tests

The test and measurement selection guide for conducted tests describes typical selection criteria for the coupling and injection points. It defines configurations and operating functions to characterize the EMC behaviour of the IC at relevant pins. The pin selection, configuration and function should be based on a typical application of the IC.

7.1.1 Pin selection for conducted RF emission and RF immunity tests

Port modules

All global pins shall be measured.

At a global driver pin the emission and immunity of the direct pin function, the crosstalk behaviour pin to core and the crosstalk behaviour port to pin can be detected.

At a global receiver pin only the crosstalk core to pin and port to pin can be detected.

If an IC has a high number of pins with the same specified functionality, it is not mandatory to measure all pins of such a functional group when a worst case assessment with respect to emission and immunity of the design has been performed and the selection is documented.

Local pin measurements are not mandatory.

Local pin measurements are optional and should be performed only on special request.

Supply modules

All supply pins shall be measured.

Core modules

The core can be measured indirectly only by crosstalk at global or local pins.

Oscillator modules

The emission of the oscillator should be measured only by crosstalk at global or local pins.

Immunity measurements can be performed optionally at the oscillator pins.

7.1.2 Coupling and injection points

IC function module	coupling and injection point			
	port pin	supply pin	core	oscillator (pin)
port module	•	•		
supply module		•		
core module	•	•		
oscillator module	•	•		(•)

(•) = test is optional

Table 14: Conducted tests: Coupling and injection points

7.1.3 Configuration for conducted RF emission tests

The following table provides necessary details to apply the selection part of the workflow for a dedicated IC. It starts with the selection of function modules with the related pin types, defines the measurement networks to be connected and it shows the operation modes and the expected coupling mechanisms in order to select the correct functional configuration and software if necessary.

coupling point				coupling mechanism				functional configuration					
				direct	indirect			without CPU (see chapter 10.1)			with CPU (see chapter 10.2)		
IC function module	pin type	measurement network (see chapter 8)	operation mode *)	functional signal	crosstalk core module to	crosstalk port module to	crosstalk oscillator module to	port module	core module	oscillator module	port module	core module	oscillator module
line driver	global	8.1.1.1	T	•				PM1			C1-S3		
			H		•				CM1			C4-S2	
			H				•			OM1			C6-S0
line receiver	global	8.1.1.2	IA		(•)				CM1			C4-S2	
sym. line driver	global	8.1.1.3	T	•				PM3			C1-S3		
			IA		•				CM1			C4-S2	
			IA				•			OM1			C6-S0
sym. line receiver	global	8.1.1.4	IA		(•)				CM1			C4-S2	
regional driver	local	8.1.1.5 config. A	T	•				PM5			C1-S3		
			H, L		•				CM1			C4-S2	
			H, L				•			OM1			C6-S0
		8.1.1.5 config. B	H, L			•			PM5		C1-S2 C1-S3		
regional Input	local	8.1.1.6	IA		(•)				CM1			C4-S2	
high side driver	local, global	8.1.1.7	T	•				PM7			C1-S3		
			H		•				CM1			C4-S2	
			H				•			OM1			C6-S0
low side driver	local, global	8.1.1.8	T	•				PM8			C1-S3		
			H		•				CM1			C4-S2	
			H				•			OM1			C6-S0
RF antenna driver	see Annex B												
RF antenna receiver	see Annex B												
supply	local, global	8.1.2	H	•				SM1			C1-S3		
			H		•				CM1			C4-S2	
			H				•			OM1			C6-S0

(•) = test is optional

Table 15: Selection guide conducted RF emission

***) Note:** T = toggle; H = static high potential, L = static low potential
IA = defined inactive, realized with internal or external pull up or pull down

7.1.4 Configuration for conducted RF immunity tests

The following table provides the necessary details to apply the selection part of the workflow for a dedicated IC. It starts with the selection of function modules with the related pin types, defines the measurement networks to be connected and it shows the operation modes in order to select the correct functional configuration and the software if necessary.

injection point				functional configuration			
				without CPU (see chapter 10.1)			with CPU (see chapter 10.2)
IC function module	pin type	test network (see chapter 8)	operation mode*)	port module	core module	oscillator module	port-, core-, oscillator modules
line driver	global	8.1.1.1	T	PM9	CM2	OM2	C10-S3
			H	PM9	CM2	OM2	C10-S3
			IA		CM3		
line receiver	global	8.1.1.2	A	PM10	CM2	OM2	C10-S3
			IA		CM3		
sym. line driver	global	8.1.1.3	T	PM11	CM2	OM2	C10-S3
			IA	PM11	CM2	OM2	C10-S3
			IA		CM3		
sym. line receiver	global	8.1.1.4	A	PM12	CM2	OM2	C10-S3
			IA		CM3		
regional driver	local	8.1.1.5 config. A	T	PM13	CM2	OM2	C10-S3
			(H)	PM13	CM2	OM2	C10-S3
			(L)	PM13	CM2	OM2	
			IA		CM3		
regional input	local	8.1.1.6	A	PM14	CM2	OM2	C10-S3
			IA		CM3		
high side driver	local, global	8.1.1.7	T	PM15	CM2	OM2	C10-S3
			(H)	PM15	CM2	OM2	C10-S3
			(L)	PM15	CM2	OM2	C10-S3
			IA		CM3		
low side driver	local, global	8.1.1.8	T	PM16	CM2	OM2	C10-S3
			(H)	PM16	CM2	OM2	C10-S3
			(L)	PM16	CM2	OM2	C10-S3
			IA		CM3		
RF antenna driver	see Annex B						
RF antenna receiver	see Annex B						
supply	local, global	8.1.2	H	SM2	CM2	OM2	C10-S3
			H	SM2	CM3	OM2	C10-S3
oscillator	local	8.1.4	T	PM9	CM2	OM2	C10-S3

(operation mode) = test is optional

Table 16: Selection guide conducted RF immunity

***) Note:** T = toggle; H = static high potential, L = static low potential
A = defined active; IA = defined inactive, realized with internal or external pull up or pull down

7.1.5 Pin selection for conducted transient pulse immunity tests

If an IC function module has a related pin it has to be checked if this pin belongs to a transient exposure category according to Table 17.

transient exposure pin category	coupling of transient disturbances	EMC pin type
1	pin directly connected to vehicle battery supply lines	global
2	pin directly connected to wiring harness	
3	pin indirectly connected to vehicle battery supply lines (via loads, expected but not mandatory specified filter or protection devices)	
4	pin indirectly connected to wiring harness I/O lines (via loads, expected but not mandatory specified filter or protection devices)	
5	pin not directly connected to vehicle wiring harness (only relevant for cross coupling on PCB, coupling networks must be adapted)	local

Table 17: Pulse affected pins according to IEC62215-3

IC function modules might be assigned to different transient exposure pin categories. For a dedicated IC only one category shall be selected for testing.

IC function module	configuration	transient exposure pin category				
		1	2	3	4	5
line driver	single, multi	-	•	•	•	-
line receiver	single, multi	-	•	•	•	-
sym. line driver		-	•	-	•	-
sym. line receiver		-	•	-	•	-
regional driver	single, multi	-	-	-	-	(•)
regional input	single, multi	-	-	-	-	(•)
high side driver	HSD*)	-	(•)	-	-	-
	LVR	-	-	-	(•)	-
	SMPS	-	-	-	(•)	-
low side driver	LSD	-	(•)	•	-	-
	SMPS	-	-	•	-	-
RF antenna driver		-	-	-	-	-
RF antenna receiver		-	-	-	-	-
supply		•	•	•	•	-
core		-	-	-	-	-
oscillator		-	-	-	-	(•)

(•) = means to be tested optionally

***)** HSD input directly tested via supply

Table 18: IC function module to transient exposure pin category matrix

module type		transient exposure pin category	connected circuitry *)	default coupling to test board **)	injection point
line driver		2	n/a	1 nF	pin
		3	device to U_{bat}	direct	at device to U_{bat}
		4	filter or protection devices	1 nF	filter or protection device
line receiver		2	n/a	1 nF	pin
		3	device to U_{bat}	direct	at device to U_{bat}
		4	filter or protection devices	1 nF	filter or protection device
symmetrical line driver		2	n/a	2 x 1 nF***)	pins
		4	filter or protection devices	2 x 1 nF***)	filter or protection device
symmetrical line receiver		2	n/a	2 x 1 nF***)	pins
		4	filter or protection devices	2 x 1 nF***)	filter or protection device
regional driver		5	n/a	10 pF	pin
regional input		5	n/a	10 pF	pin
high side driver	HSD	2	load	1 nF	pin
	SMPS, LVR	4	output circuitry		at connected circuitry
low side driver	LSD	2	load	1 nF	pin
	LSD SMPS	3	load, input circuitry	direct	at load or connected circuitry
RF antenna driver		n/a			
RF antenna receiver		n/a			
Supply		1	n/a	direct	pin
		2	n/a	1 nF	pin
		3	device to U_{bat} optional: maximum ratings limitation circuitry	direct	input of connected circuitry
		4	filter or protection devices	1 nF	filter or protection device
Core		n/a			
oscillator		5	default circuitry according to data sheet	10 pF	pin

Table 19: Transient immunity test circuit selection

*) **Note:** Mandatory components are always populated for all configurations.

) **Note: Coupling capacity shall be adapted to value according to data sheet for proper functionality.

***) Note:** Multi point injection

7.1.6 Configuration for conducted transient pulse immunity tests

The following table provides the necessary details to apply the selection part of the workflow for a dedicated IC. It starts with the selection of function modules with the related pin types, defines the measurement networks to be connected and it shows the operation modes in order to select the correct functional configuration and the software if necessary.

injection point				functional configuration			
				without CPU (see chapter 10.1)			with CPU (see chapter 10.2)
IC function module	pin type	test network (see chapter 8)	operation mode*)	port module	core module	oscillator module	port-, core-, oscillator modules
line driver	global	8.1.1.1	T	PM9	CM2	OM2	C10-S3
			H	PM9	CM2	OM2	C10-S3
			IA		CM3		
line receiver	global	8.1.1.2	A	PM10	CM2	OM2	C10-S3
			IA		CM3		
sym. line driver	global	8.1.1.3	T	PM11	CM2	OM2	C10-S3
			IA	PM11	CM2	OM2	C10-S3
			IA		CM3		
sym. line receiver	global	8.1.1.4	A	PM12	CM2	OM2	C10-S3
			IA		CM3		
regional driver	local	8.1.1.5 config. A	T	PM13	CM2	OM2	C10-S3
			(H)	PM13	CM2	OM2	C10-S3
			(L)	PM13	CM2	OM2	
			IA		CM3		
regional input	local	8.1.1.6	A	PM14	CM2	OM2	C10-S3
			IA		CM3		
high side driver	local, global	8.1.1.7	T	PM15	CM2	OM2	C10-S3
			(H)	PM15	CM2	OM2	C10-S3
			(L)	PM15	CM2	OM2	C10-S3
			IA		CM3		
low side driver	local, global	8.1.1.8	T	PM16	CM2	OM2	C10-S3
			(H)	PM16	CM2	OM2	C10-S3
			(L)	PM16	CM2	OM2	C10-S3
			IA		CM3		
RF antenna driver	Annex B						
RF antenna receiver	Annex B						
supply – sub net	local, global	8.1.2	H	SM2	CM2	OM2	C10-S3
			H	SM2	CM3	OM2	C10-S3
supply – power net	global	8.1.2	H	SM2	CM2	OM2	C10-S3
oscillator	local	8.1.4	T	PM9	CM2	OM2	C10-S3

(operation mode) = test is optional

Table 20: Selection guide conducted transient immunity

***) Note:** T = toggle; H = static high potential, L = static low potential
A = defined active; IA = defined inactive, realized with internal or external pull up or pull down

7.1.7 Pin selection for unpowered system level ESD tests

The purpose of *system level* ESD packaging and handling test is to characterize protection capability for global pins of integrated circuits including mandatory components.

All global pins shall be tested according to the IC or customer specification vs. GND only.

IC level ESD packaging and handling tests on all pins (global and local) shall guarantee sufficient protection capability for safe and proper handling of semiconductor components (IC- manufacturing, - transport, - assembly on PCB). These tests and requirements are described in [15, 16, 17, 18]. They are part of the IC specification according to AECQ100 and therefore not considered in this specification.

7.1.8 Configuration for unpowered system level ESD tests

For unpowered system level ESD tests on IC pins an IC test configuration is not necessary.

7.2 Radiated tests

7.2.1 Criteria for performing radiated emission and immunity tests

Emission:

- the IC has a CPU, or
- the IC has a digital logic FFU or an oscillator module with an operating frequency higher than 10 MHz and a package diagonal dimension greater than 25 mm

Immunity:

- the IC has an analog FFU as sensing element working with electrical or magnetic fields, or
- the IC has an analog or digital FFU with charge coupled devices (CCD) for filtering

7.2.2 Test configuration for radiated emission

coupling structure	test setup	functional configuration	
entire IC	(G)TEM-cell chapter 9.2 or IC stripline chapter 9.3	**without CPU**	**with CPU**
		CM1	C1-S2

Table 21: Selection guide radiated emission

7.2.3 Test configuration for radiated immunity

injection structure	test setup	functional configuration	
entire IC	(G)TEM-cell chapter 9.2 or IC stripline chapter 9.3	**without CPU**	**with CPU**
		CM2	C10-S3
		CM3	C11-S3

Table 22: Selection guide radiated immunity

8 Test and measurement networks

8.1 Emission and immunity tests

This chapter describes the coupling, injection and monitoring networks for conducted emission measurements and immunity tests. All unused pins shall be set into a defined state and configuration according to the IC data sheet. The electrical characteristics (power dissipation, voltage, current, frequency properties) of the passive components on the test PCB shall meet the functional and test requirements.

The trace impedance between the RF connector and coupling network and to the pin under test shall be 50 Ω.

8.1.1 Port module

8.1.1.1 Line driver

For common line drivers the following networks shall be used, for special line drivers type **LIN** refer to specification [20].

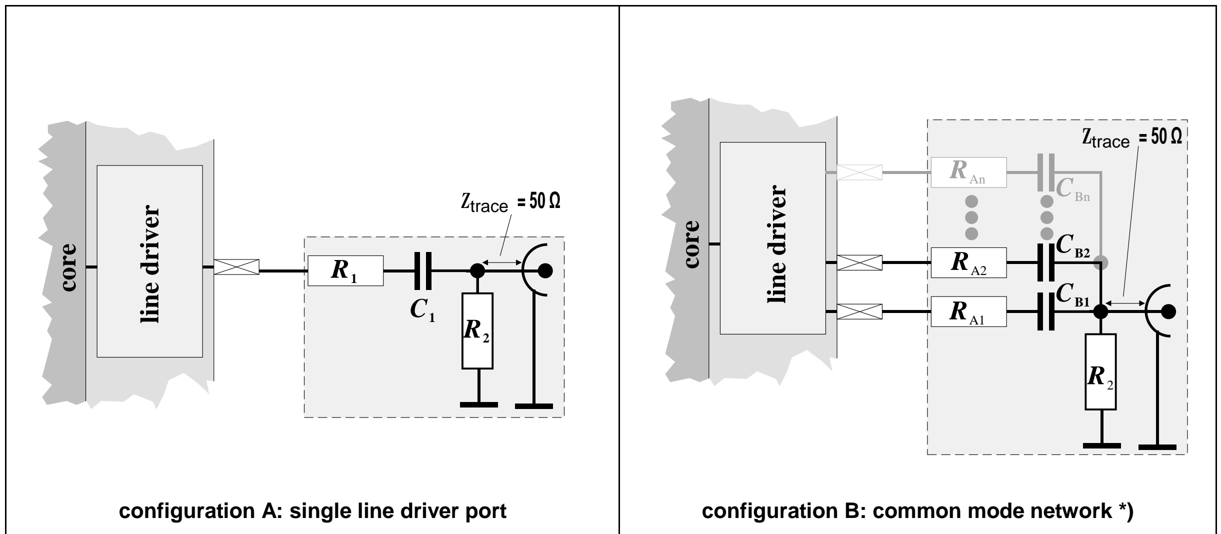


Figure 9: Test and measurement networks for line driver

***) Note:** Use circuit B for common mode testing only (e.g. airbag squib driver, sensors, application acc. to Annex F of IEC 61967-4)

component variation for RF emission test setup	
item	**value**
R_1	120 Ω
R_2	51 Ω
C_1	6.8 nF or less as max. load capacitance according to IC data sheet
$R_{A1}= R_{A2}=...=R_{An}$	$R_A\|_{\pm 5\%} = 120\Omega \cdot n$ n = number of *Line Drivers* select a resistor according to resistor standard set within tolerance of 5%
$C_{B1}= C_{B2}=...= C_{Bn}$	$C_B\|_{\pm 5\%} = \frac{C_1}{n}$ n = number of *Line Drivers* Select a capacitor according to capacitor standard set within tolerance of 5%

component variation for RF immunity test setup	
item	**value**
R_1	0 Ω as default, up to 100 Ω for load current limitation according to data sheet
R_2	open
C_1	6.8 nF or less as max. load capacitance according to IC data sheet
$R_{A1}= R_{A2}=\ldots=R_{An}$	$R_A\|_{\pm5\%} = R_1 \cdot n$ *n* = number of *Line Drivers* select a resistor according to resistor standard set within tolerance of 5%
$C_{B1}= C_{B2}=\ldots= C_{Bn}$	$C_B\|_{\pm5\%} = \frac{C_1}{n}$ *n* = number of *Line Drivers* select a capacitor according to capacitor standard set within tolerance of 5%

component variation for transients test setup	
item	**value**
R_1	0 Ω as default
R_2	Open
C_1	1 nF or less as max. load capacitance according to IC data sheet
$R_{A1}= R_{A2}=\ldots=R_{An}$	$R_A\|_{\pm5\%} = R_1 \cdot n$ *n* = number of line drivers select a resistor according to resistor standard set within tolerance of 5%
$C_{B1}= C_{B2}=\ldots= C_{Bn}$	$C_B\|_{\pm5\%} = \frac{C_1}{n}$ *n* = number of line drivers select a capacitor according to capacitor standard set within tolerance of 5%
filter or protection devices	acc. to IC data sheet or application note

Table 23: Network for emission, immunity and transients tests for IC module line driver

8.1.1.2 Line receiver

For common line receivers the following networks shall be used, for special line receivers type **LIN** refer to specification [20].

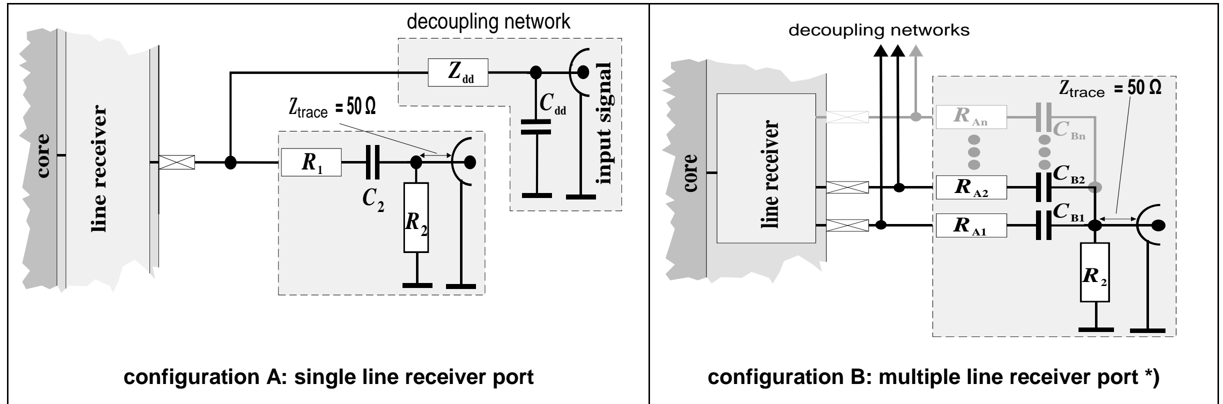


Figure 10: Test and measurement networks for line receiver

***) Note**: Use circuit B, if more than one driver are tested simultaneously of a multiple line receiver port.

component variation for RF emission test setup
for receiver ports emission tests are not mandatory

component variation for RF immunity test setup	
item	**value**
Z_{dd}	> 400 Ω
C_{dd}	10 nF or acc. to max. frequency of input signal
R_1	0 Ω as default, up to 100 Ω for load current limitation according data sheet
R_2	open
C_2	6,8 nF or less as max. load capacitance according to IC data sheet
$R_{A1}= R_{A2}=...= R_{An}$	$R_A\|_{\pm5\%} = R_1 \cdot n$ *n* = number of line drivers Select a resistor according to resistor standard set within tolerance of 5%
$C_{B1}= C_{B2}=...= C_{Bn}$	$C_B\|_{\pm5\%} = \frac{C_2}{n}$ *n* = number of line drivers select a capacitor according to capacitor standard set within tolerance of 5%

component variation for transients test setup	
item	**value**
Z_{dd}	> 400 Ω
C_{dd}	10 nF or acc. to max. frequency of input signal
R_1	0 Ω as default
R_2	open
C_2	1 nF or less as max. load capacitance according to IC data sheet
$R_{A1}= R_{A2}=...= R_{An}$	$R_A\|_{\pm5\%} = R_1 \cdot n$ *n* = number of line drivers select a resistor according to resistor standard set within tolerance of 5%
$C_{B1}= C_{B2}=...= C_{Bn}$	$C_B\|_{\pm5\%} = \frac{C_2}{n}$ *n* = number of line drivers select a capacitor according to capacitor standard set within tolerance of 5%
filter or protection devices	acc. to IC data sheet or application note

Table 24: Network for immunity and transients tests for IC module line receiver

8.1.1.3 Symmetrical line driver

For common symmetrical line drivers the following networks shall be used, for special symmetrical line drivers type **CAN** refer to specification [19].

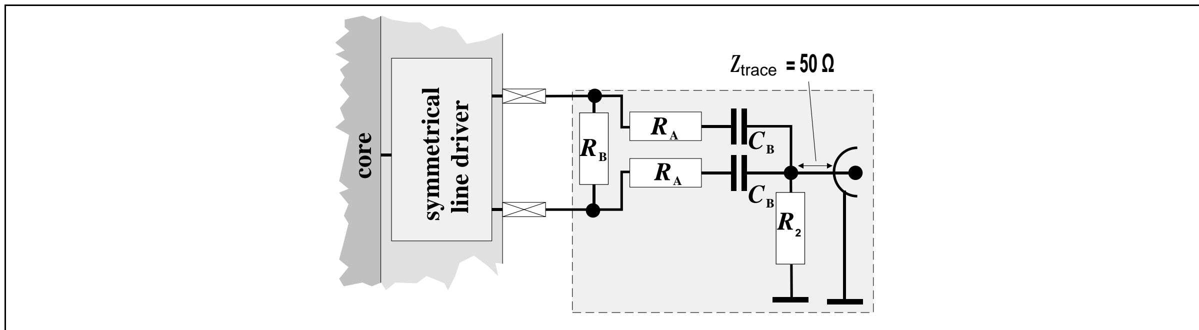


Figure 11: Test and measurement networks for symmetrical line driver

component variation for RF emission test setup	
item	**value**
R_B	according to bus specification*)
R_A	240 Ω Note: the resistors shall be matched with tolerance better than 0.1%
R_2	51 Ω
C_B	6,8 nF or max. load capacitance according to IC data sheet Note: the capacitors shall be matched with tolerance better than 1%

component variation for RF immunity test setup	
item	**value**
R_B	according to bus specification*)
R_A	0 Ω as default, up to 100 Ω for load current limitation according to data sheet Note: the resistors shall be matched with tolerance better than 0.1%
R_2	open
C_B	6,8 nF or less as max. load capacitance according to IC data sheet Note: the capacitors shall be matched with tolerance better than 1%

component variation for transients test setup	
item	**value**
R_B	according to bus specification*)
R_A	0 Ω as default
R_2	open
C_B	1 nF (or less as max. load capacitance according to data sheet) Note: the capacitors shall be matched with tolerance better than 1%
filter or protection devices	acc. to IC data sheet or application note

Table 25: Network for emission, immunity and transients tests for IC module symmetrical line driver

***) Note:** Termination is not part of the test network, but may be needed for the symmetrical line driver

8.1.1.4 Symmetrical line receiver

For common symmetrical line drivers the following networks shall be used, for special symmetrical line receivers type **CAN** refer to specification [19].

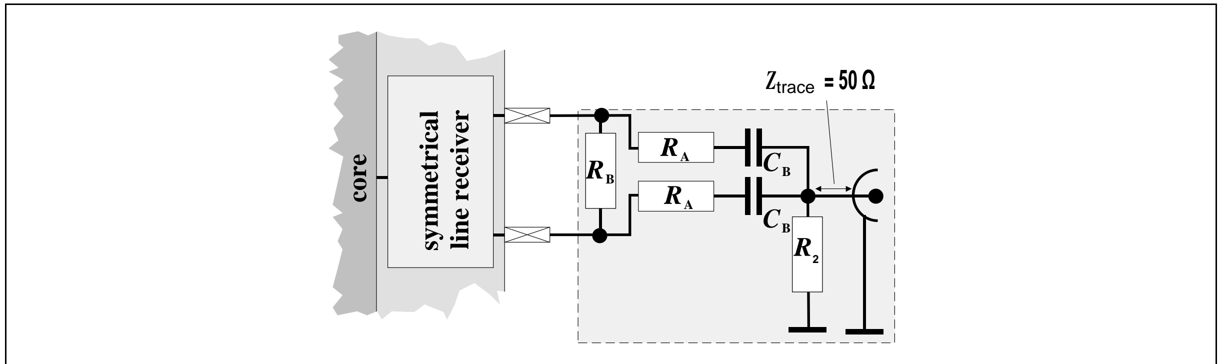


Figure 12: Test and measurement networks for symmetrical line receiver

component variation for RF emission test setup
for symmetrical line receiver ports emission tests are not mandatory

component variation for RF immunity test setup	
item	**value**
R_B	according to bus specification*)
R_A	0 Ω as default, up to 100 Ω for load current limitation according to data sheet *Note: the resistors shall be matched with tolerance better than 0,1%*
R_2	open
C_B	6,8 nF or less as max. load capacitance according to IC data sheet *Note: the capacitors shall be matched with tolerance better than 1%*

component variation for transients test setup	
item	**value**
R_B	according to bus specification*)
R_A	0 Ω as default, up to 100 Ω for load current limitation according to data sheet *Note: the resistors shall be matched with tolerance better than 0,1%*
R_2	open
C_B	1 nF (or less as max. load capacitance according to data sheet) *Note: the capacitors shall be matched with tolerance better than 1%*
filter or protection devices	acc. to IC data sheet or application note

Table 26: Network for immunity and transients tests for IC module symmetrical line receiver

***) Note:** Termination is not part of the test network, but may be needed for the symmetrical line receiver

8.1.1.5 Regional driver

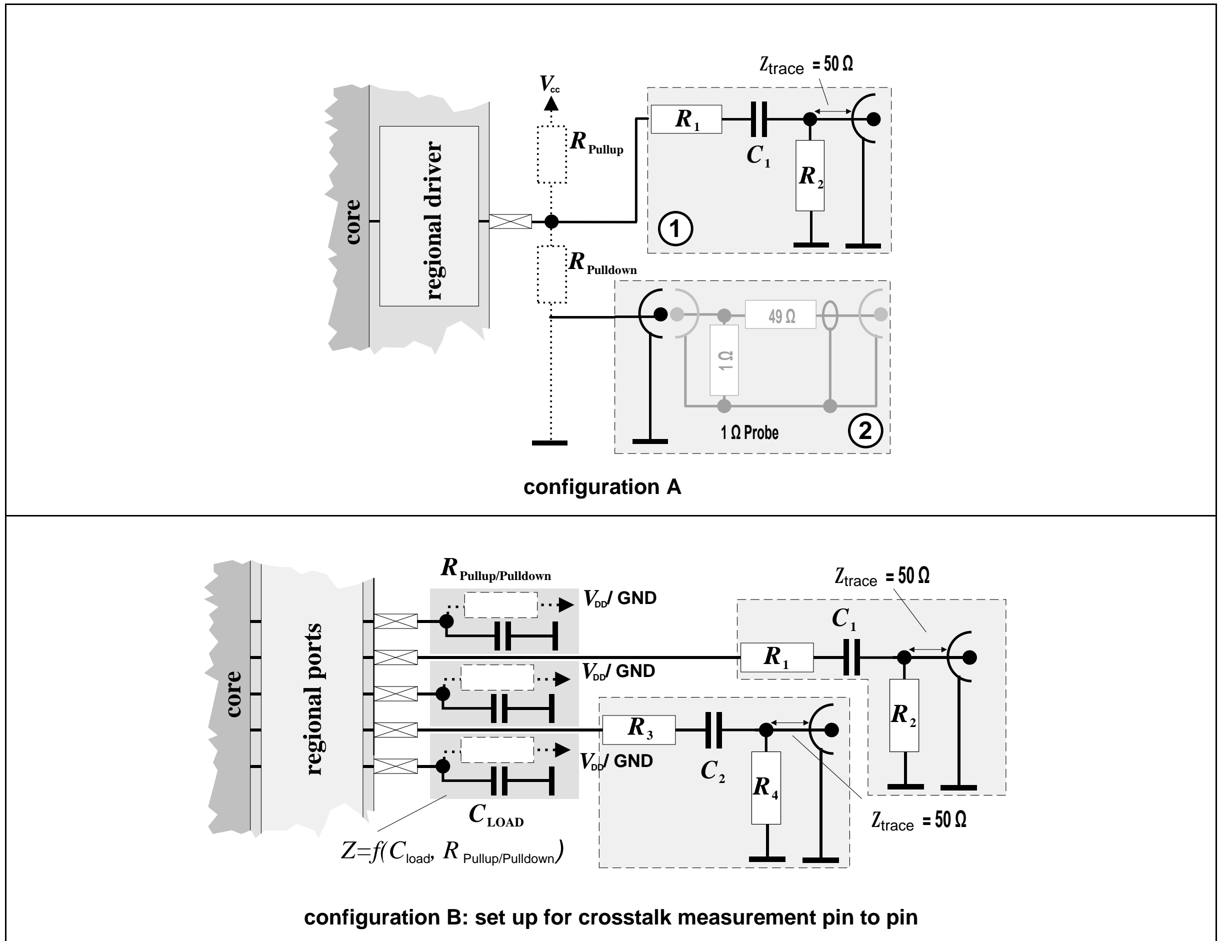


Figure 13: Test and measurement networks for regional driver

general network component variation	
item	**value**
R_{Pullup}	digital signal: according to IC data sheet (typical value), if it is needed for external pull up (default 3300 Ω) analog signal: signal connection to functional required circuit
$R_{Pulldown}$	according to IC data sheet (typical value)
C_{load}	max. load capacitance according to IC data sheet
or	
$Z = f\,(C_{load}, R_{Pullup/Pulldown})$	real loads (e.g. memory) or passive substitution networks according to IC data or application sheet

component variation for RF emission test setup	
item	**value**
R_1, R_3	120 Ω
R_2, R_4	51 Ω
C_1, C_2	6,8 nF or less as max. load capacitance according to IC data sheet
test network	“1” if $R_{pullup\text{-}down} \leq 30$ Ω or static mode (DC)
	“2” if $R_{pullup\text{-}down} > 30$ Ω

component variation for RF immunity test setup	
item	**value**
R_1, R_3	0 Ω as default, up to 100 Ω for load current limitation according to data sheet
R_2, R_4	open
C_1, C_2	6,8 nF or less as max. load capacitance according to IC data sheet
test network 2	shorted

component variation for transients test setup	
item	**value**
R_1, R_3	0 Ω as default, up to 100 Ω for load current limitation according to data sheet
R_2, R_4	open
C_1, C_2	10 pF or less as max. load capacitance according to IC data sheet
test network 2	shorted

Table 27: Network for emission, immunity and transients tests for IC module regional driver

8.1.1.6 Regional input

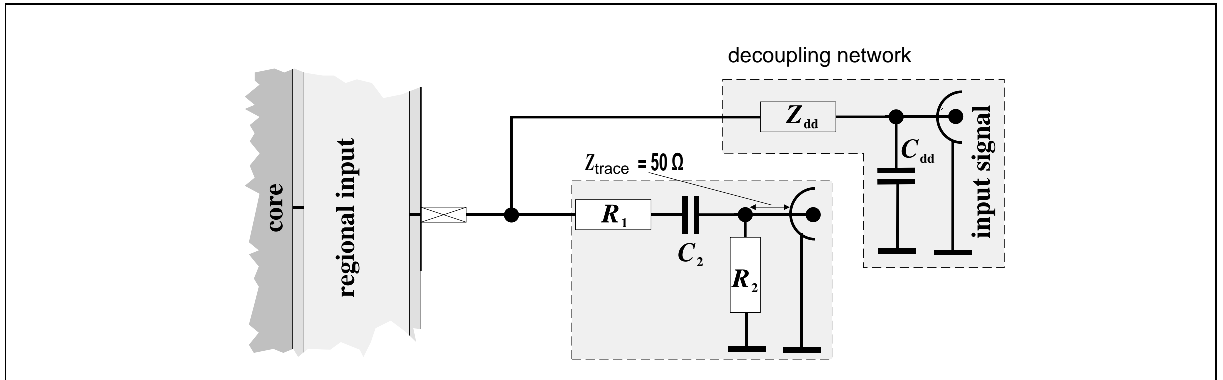


Figure 14: Test and measurement networks for regional input

component variation for RF emission test setup
for input ports emission tests are not mandatory

component variation for RF immunity test setup	
item	**value**
Z_{dd}	> 400 Ω
C_{dd}	10 nF or acc. to max. frequency of input signal
R_1	0 Ω as default, up to 100 Ω for load current limitation according to data sheet
R_2	open
C_2	6,8 nF or less as max. load capacitance according to IC data sheet)

component variation for transients test setup	
item	**value**
Z_{dd}	> 400 Ω
C_{dd}	10 nF or acc. to max. frequency of input signal
R_1	0 Ω as default, up to 100 Ω for load current limitation according to data sheet
R_2	open
C_2	10 pF(or less as max. load capacitance according to IC data sheet)

Table 28: Network for immunity and transients tests for IC module regional input

8.1.1.7 High side driver

- Emission: In addition to IEC61967-4, the impedance determining 150 Ω network and the load impedance are decoupled by a 5 µH coil (L_{BAN}), to get results independent from the load impedance.
- Immunity: In addition to IEC62132-4, a broadband artificial network (BAN) consisting of a 5 µH coil (L_{BAN}) and a 150 Ω matching network (R_{BAN} , C_{BAN}) for impedance fixing is added.

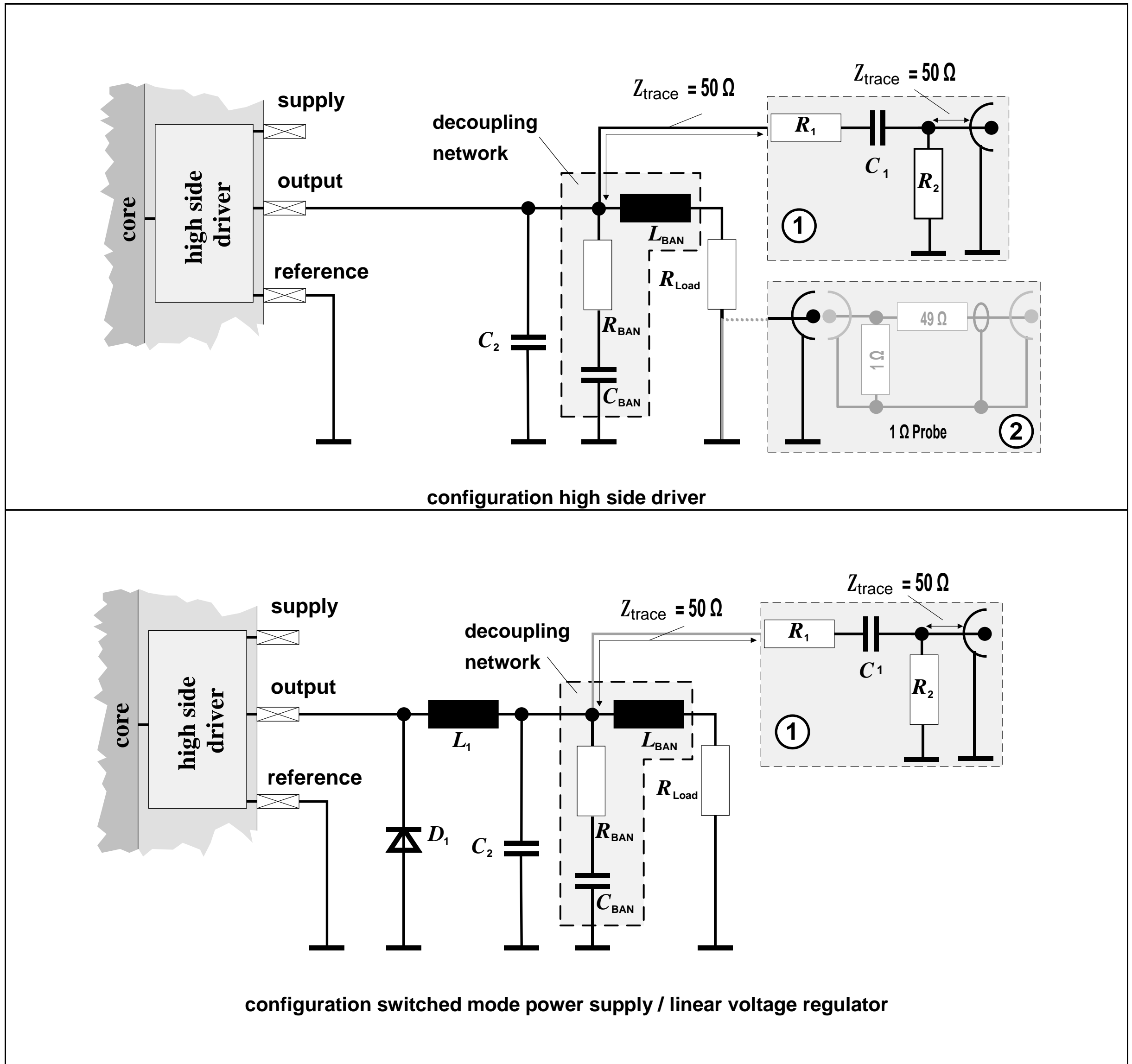


Figure 15: Test and measurement networks for high side driver

general network component variation			
item	**value for high side driver**	**value for linear voltage regulator**	**value for switched mode power supply (buck converter)**
L_{BAN}	5 µH (independent of load current, no saturation effects, $Z_{LBAN\ (5\text{-}1000MHz)} \geq 150\ \Omega$)		
L_1	shorted	shorted	acc. to IC data sheet
D_1	open	open	acc. to IC data sheet
C_2	open	acc. to IC data sheet	acc. to IC data sheet
R_{load}	according to I_{meas} *) $I_{meas} = \sqrt{\frac{\Delta T}{R_{th} \cdot R_{on,150°C}}}$ (ΔT = 65 K, $I_{meas} \leq 10$ A)	according to I_{meas} *) I_{meas} = 80 % of I_{nom}	according to I_{meas} *) I_{meas} = 80% of I_{nom}

***) Note:** The IC dissipation power $P_{dissipation}$ is basically limited by R_{th} of the housing and the maximum temperature T_{max} of the semiconductor at a maximum ambient temperature T_{amb} according to data sheet. With the definitions T_{max} = 150°C at T_{amb} = 85°C a ΔT = 65K is given. The typical power dissipation is additionally given by $R_{on,150°C}$ and a typical *load current* I_{load}: $P_{dissipation} = I_{load}^2 \cdot R_{on,150°C}$ and $\Delta T = P_{dissipation} \cdot R_{th}$.

component variation for RF emission test setup			
item	**value for high side driver**	**value for linear voltage regulator**	**value for switched mode power supply (buck converter)**
R_1	120 Ω	120 Ω	120 Ω
R_2	51 Ω	51 Ω	51 Ω
C_1	6,8 nF	6,8 nF	6,8 nF
test network 1	$R_{load} \leq 30\ \Omega$ or static mode (DC)	$R_{load} \leq 30\ \Omega$ or static mode (DC)	$R_{load} \leq 30\ \Omega$ or static mode (DC)
test network 2	$R_{load} > 30\ \Omega$, L_{BAN} short	n/a	n/a
R_{BAN}	open	open	open
C_{BAN}	open	open	open

component variation for RF immunity test setup			
item	**value for high side driver**	**value for linear voltage regulator**	**value for switched mode power supply (buck converter)**
R_1	0 Ω as default, up to 100 Ω for load current limitation according to data sheet		
R_2	open	open	open
C_1	6,8 nF or less as max. load capacitance according to IC data sheet		
R_{BAN}	150 Ω	150 Ω	150 Ω
C_{BAN}	6,8 nF	6,8 nF	6,8 nF

component variation for transients test setup			
item	value for high side driver	value for linear voltage regulator	value for switched mode power supply (buck converter)
R_1	0 Ω as default, up to 100 Ω for load current limitation according to data sheet		
R_2	open	open	open
C_1	*global pin*: 1 nF (or less as max. load capacitance according to IC data sheet) *local pin*: 10 pF(or less as max. load capacitance according to IC data sheet)		
R_{BAN}	150 Ω	150 Ω	150 Ω
C_{BAN}	6,8 nF	6,8 nF	6,8 nF

Table 29: Network for emission, immunity and transients tests for IC module high side driver

8.1.1.8 Low side driver

- Emission: In addition to IEC61967-4, the impedance determining 150 Ω network and the load impedance are decoupled by a 5 µH coil (L_{BAN}), to get results independent from the load impedance.
- Immunity: In addition to IEC62132-4, a broadband artificial network (BAN) consisting of a 5 µH coil (L_{BAN}) and a 150 Ω matching network (R_{BAN} , C_{BAN}) for impedance fixing is added.

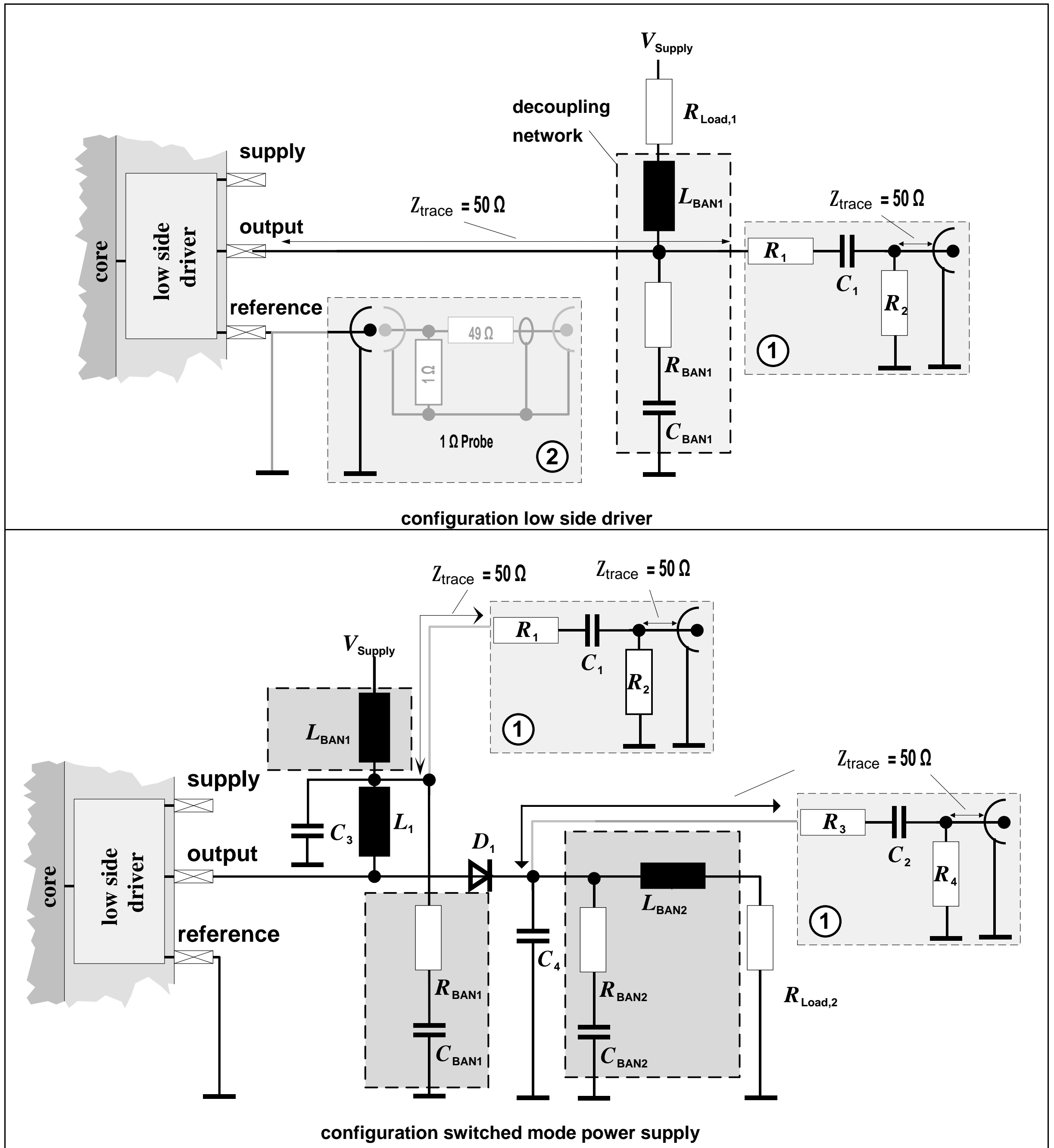


Figure 16: Test and measurement networks for low side driver

general network component variation		
item	**value for low side driver**	**value for switched mode power supply (boost converter)**
L_1	shorted	acc. to IC data sheet
D_1	shorted	acc. to IC data sheet
C_3	open	acc. to IC data sheet
C_4	open	acc. to IC data sheet
$R_{load,1}$ **)	according to I_{meas} *) $I_{meas} = \sqrt{\frac{\Delta T}{R_{th} \cdot R_{on,150°C}}}$ (ΔT = 65 K, $I_{meas} \leq$ 10 A)	n/a
$R_{load,2}$	n/a	according to I_{meas} I_{meas} = 80% of I_{nom}

***) Note:** The IC dissipation power $P_{dissipation}$ is basically limited by R_{th} of the housing and the maximum temperature T_{max} of the semiconductor at a maximum ambient temperature T_{amb} according to data sheet. With the definitions T_{max} = 150°C at T_{amb} = 85°C a ΔT = 65K is given. The typical power dissipation is additionally given by $R_{on,150°C}$ and a typical *load current* I_{load}: $P_{dissipation} = I_{load}^2 \cdot R_{on,150°C}$ and $\Delta T = P_{dissipation} \cdot R_{th}$.

****) Note:** If a specific load (e.g. solenoid) is defined and available it shall be used.

component variation for RF emission test setup		
item	**value for low side driver**	**value for switched mode power supply (boost converter)**
L_{BAN1}	5 µH (independent of load current, no saturation effects, $Z_{LBAN\ (5\text{-}1000MHz)} \geq$ 150 Ω)	
L_{BAN2}	shorted	5 µH
R_1, R_3	120 Ω	120 Ω
R_2, R_4	51 Ω	51 Ω
C_1, C_2	6,8 nF	6,8 nF
test network 1	$R_{load} \leq$ 30 Ω or static mode (DC)	$R_{load} \leq$ 30 Ω or static mode (DC)
test network 2	R_{load} > 30 Ω	n/a
R_{BAN1}, R_{BAN2}	open	open
C_{BAN1}, C_{BAN2}	open	open

component variation for RF immunity test setup		
item	**value for low side driver**	**value for switched mode power supply (boost converter)**
L_{BAN1}	5 µH (independent of load current, no saturation effects, $Z_{LBAN\ (5\text{-}1000MHz)} \geq$ 150 Ω)	
L_{BAN2}	shorted	5 µH
R_1, R_3	0 Ω as default, up to 100 Ω for load current limitation according to data sheet	
R_2, R_4	open	open
C_1, C_2	6,8 nF or less as max. load capacitance according to IC data sheet	
R_{BAN1}, R_{BAN2}	150 Ω	150 Ω
C_{BAN1}, C_{BAN2}	6,8 nF	6,8 nF

component variation for transients test setup (power net)		
item	**value for low side driver**	**value for switched mode power supply (boost converter)**
L_{BAN1}...L_{BANx}	open (supplied via transient test generator)	
R_1, R_3	0 Ω as default, up to 100 Ω for load current limitation according to data sheet	
R_2, R_4	open	open
C_1, C_2	short	short
R_{BAN1}...R_{BANx}	open	open
C_{BAN1}...C_{BANx}	open	open
filter or protection devices	acc. to IC data sheet or application note	

component variation for transients test setup (sub supply net)		
item	**value for low side driver**	**value for switched mode power supply (boost converter)**
L_{BAN1}	5 µH (independent of load current, no saturation effects, $Z_{LBAN\ (5\text{-}1000MHz)}$ ≥ 150 Ω)	
L_{BAN2}	shorted	5 µH (as L_{BAN1})
R_1, R_3	0 Ω as default, up to 100 Ω for load current limitation according to data sheet	
R_2, R_4	open	open
C_1, C_2	*global:* 1 nF	*global:* 1 nF
	local: 10 pF	*local:* 10 pF
R_{BAN1}...R_{BANx}	open	open
C_{BAN1}...C_{BANx}	open	open
filter or protection devices	acc. to IC data sheet or application note	

Table 30: Network for emission and immunity tests for IC module low side driver

8.1.1.9 RF antenna driver

RF drivers, driving radio frequency signals into an antenna matching circuitry or a 50 Ω impedance matching circuitry, are classified as 'local' with respect to EMC. No conducted test methods are applicable. RF tests on ICs with this pin type are described in Annex B.

LF signal drivers shall be tested as line drivers described in chapter 8.1.1.1.

ESD test network for this pin type connected to a line connector via matching circuitry is described in Chapter 8.2.1.

8.1.1.10 RF antenna receiver

RF receivers, receiving radio frequency signals from an antenna matching circuitry or a 50 Ω impedance matching circuitry, are classified as 'local' with respect to EMC. No conducted test methods are applicable. RF tests on ICs with this pin type are described in Annex B.

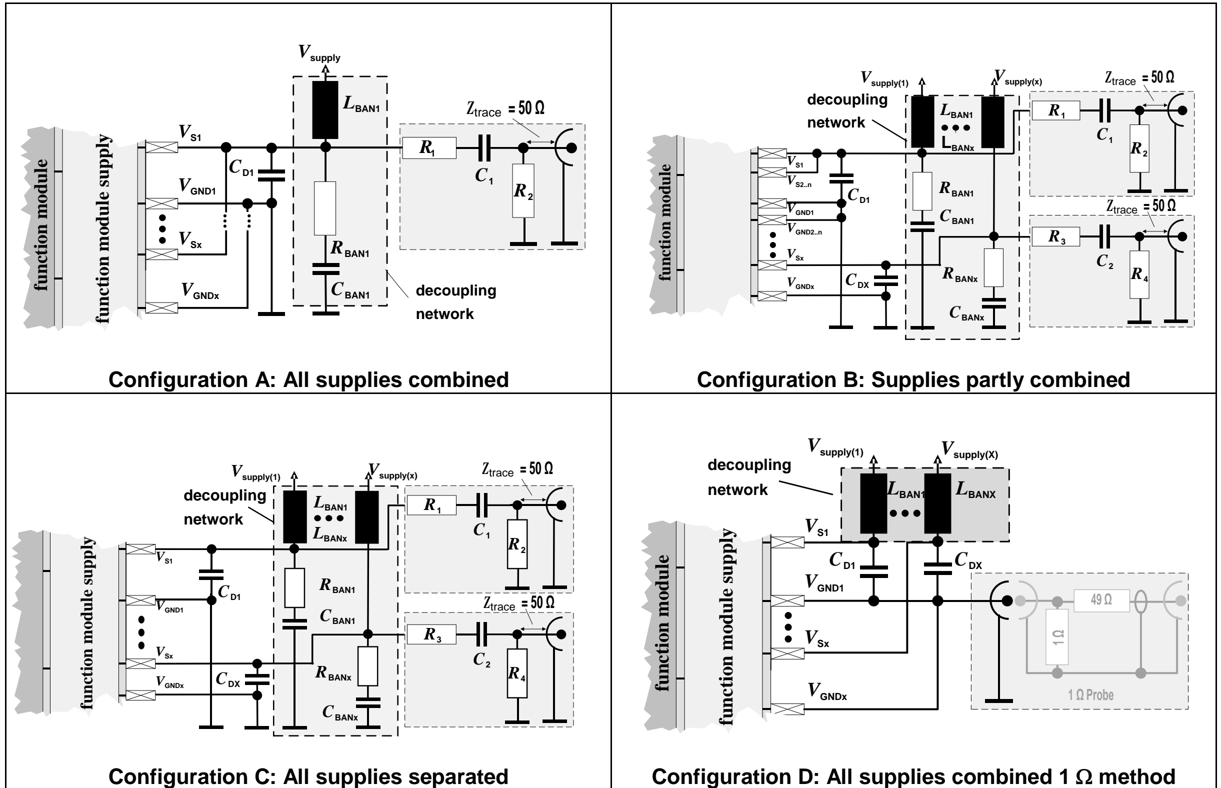
LF signal receivers shall be tested as line receivers described in chapter 8.1.1.2.

ESD test network for this pin type connected to a line connector via matching circuitry is described in Chapter 8.2.1.

8.1.2 Supply module

RF Emission: In addition to IEC61967-4, the impedance determining 150 Ω network and the load impedance are decoupled by a 5 µH coil (L_{BAN}), to get results independent from the load impedance.

RF Immunity: In addition to *IEC62132-4*, a broadband artificial network (BAN) consisting of a 5 µH coil (L_{BAN}) and a 150 Ω matching network (R_{BAN} , C_{BAN}) for impedance fixing is added.



Configuration A: All supplies combined

Configuration B: Supplies partly combined

Configuration C: All supplies separated

Configuration D: All supplies combined 1 Ω method

Figure 17: Test and measurement network supply modules

component variation for RF emission test setup	
item	**value**
$C_{D1} \ldots C_{Dx}$	Supply Decoupling Capacitor acc. to IC data sheet
R_1, R_3	120 Ω
R_2, R_4	51 Ω
C_1, C_2	6,8 nF or less as max. load capacitance according to IC data sheet
$L_{BAN1} \ldots L_{BANx}$	5 µH (independent of load current, no saturation effects, $Z_{LBAN\ (5\text{-}1000MHz)} \geq 150\ \Omega$)

component variation for RF immunity test setup	
item	**value**
$C_{D1} \ldots C_{Dx}$	supply decoupling capacitor acc. to IC data sheet
R_1, R_3	0 Ω as default, up to 100 Ω for load current limitation according to data sheet
R_2, R_4	open
C_1, C_2	6,8 nF or less as max. load capacitance according to IC data sheet
$R_{BAN1} \ldots R_{BANx}$	150 Ω
$C_{BAN1} \ldots C_{BANx}$	6,8 nF
$L_{BAN1} \ldots L_{BANx}$	5 µH (independent of load current, no saturation effects, $Z_{LBAN\ (5\text{-}1000MHz)} \geq 150\ \Omega$)

component variation for transients test setup (power net)	
item	**value**
$C_{D1} \ldots C_{Dx}$	supply decoupling capacitor acc. to IC data sheet
R_1, R_3	0 Ω as default, up to 100 Ω for load current limitation according to data sheet
R_2, R_4	open
C_1, C_2	short
$R_{BAN1} \ldots R_{BANx}$	open
$C_{BAN1} \ldots C_{BANx}$	open
$L_{BAN1} \ldots L_{BANx}$	open (supplied via transient test generator)
filter or protection devices	acc. to IC data sheet or application note

component variation for transients test setup (sub supply net)	
item	**value**
R_1, R_3	0 Ω as default, up to 100 Ω for load current limitation according to data sheet
R_2, R_4	open
C_1, C_2	*global:* 1 nF
	local: 10 pF
$R_{BAN1} \ldots R_{BANx}$	open
$C_{BAN1} \ldots C_{BANx}$	open
$L_{BAN1} \ldots L_{BANx}$	5 µH (independent of load current, no saturation effects, $Z_{LBAN\ (5\text{-}1000MHz)} \geq 150\ \Omega$)
filter or protection devices	acc. to IC data sheet or application note

Table 31: Network for emission and immunity tests for IC module supply

8.1.3 Core module

The conducted emission and immunity of the core module cannot be measured directly. All emission or immunity tests shall be performed by using cross talk effects between

- core and supply
- core and port
- core and oscillator

8.1.4 Oscillator module

The emission of the oscillator should be measured only by crosstalk at global or local pins. Immunity measurements can be performed optionally directly at the oscillator.

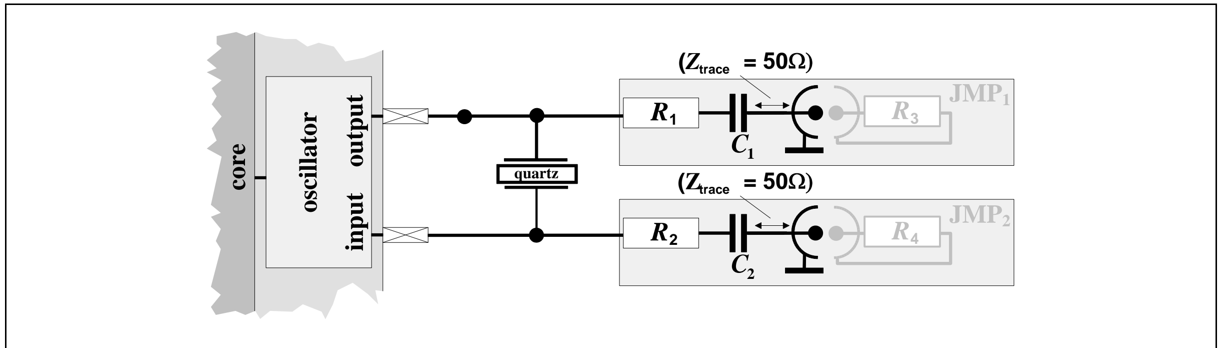


Figure 18: Test and measurement networks oscillator module

component variation for RF emission test setup
for oscillator modules emission tests are not required

component variation for RF immunity test setup	
item	**value**
R_1, $R2$	0 Ω
C_1, C_2	oscillator capacitors: 10 pF or maximum according to data sheet
JMP_1, JMP_2	jump plug (R_3=R_4=50 Ω) connected to the not used injection point

component variation for transients test setup	
item	**value**
R_1, R_2	0 Ω
C_1, C_2	Oscillator capacitors: 10 pF or maximum according to data sheet
JMP_1, JMP_2	Jump plug (R_3=R_4=50 Ω) connected to the not used injection point

Table 32: Network for immunity tests for IC module oscillator

8.2 ESD test

8.2.1 Test network for unpowered system level ESD tests

ESD test on global pins shall be performed according to the following test network. All GND pins shall be shorted on the test board. All other pins can be left open.

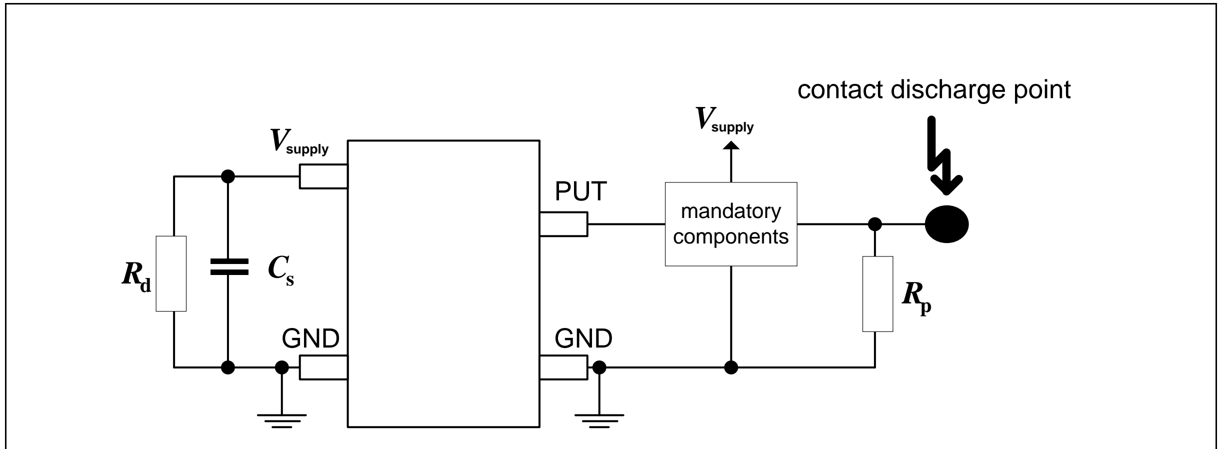


Figure 19: Test network for unpowered system ESD test on global pin

ESD network for global supply pin	
item	**value**
C_s capacitor for decoupling purpose	100 nF if no other value is specified
R_d discharge resistor parallel to decoupling capacitance V_{supply} to GND for self-discharging after ESD test and avoids pre-charging of the pin under test by the ESD gun before testing (see Figure 19)	≥ 220 kΩ
mandatory components	as specified acc. to data sheet
additional external components	as described in application note, test specification, test report, etc.

Table 33: External components global supply pin

ESD network for global port pin	
item	**value**
R_p discharge resistor parallel to pin under test to avoid pre-charging of the pin under test by the ESD gun before testing and to discharge the pin under test after ESD testing (see Figure 19)	≥ 220 kΩ
mandatory components	as specified acc. to data sheet
additional external components	as described in application note, test specification, test report, etc.

Table 34: External components global port pin

9 Test setup

9.1 Signal decoupling for stimulus and monitoring

9.1.1 Stimulus setup

The stimulus signals and setup should not affect the measurements. Following topics should be considered to reach this requirement:

- The reference ground on PCB for functionality, RF and transient test signals should be checked and optimized for current separation.
- For external clock injection coaxial cables with appropriate RF connector types, short traces to the clock input pin(s) and separate ground routing shall be used. The emission of the unpowered test board with active external clock has to be verified.
- For emission measurements the signal-to-disturbance margin of the stimulus signal can be reduced to the minimum stimulus signal definition parameters: maximum rise and fall times, minimum signal amplitude, maximum source impedance.

9.1.2 DUT Monitoring

The pins to be monitored shall be specified in the dedicated IC EMC test specification.

Generally, all DUT functions, which are decided to be monitored, have to be checked. For conducted RF immunity and transient tests the DUT functions can be monitored directly or indirectly at output ports. For radiated immunity tests the distinction between direct and indirect monitoring is not possible. All monitored signals shall be within the failure criteria of the IC EMC test specification.

direct monitoring: Monitoring at the pin under test

indirect monitoring: All other monitoring

RF decoupling: RF filter necessary to prevent the monitoring device from the disturbance.

transients decoupling: Signal decoupling by fibre optic conversion might be necessary to prevent the monitoring device from the disturbance.

monitoring device: The monitoring can be realized e.g. by a microcontroller (µC) test application with a cycling test program, an oscilloscope with a programmable signal tolerance mask, a multimeter.

An example how the monitored signals can be combined to a logical sum "within specification or out of specification" is shown in Figure 20.

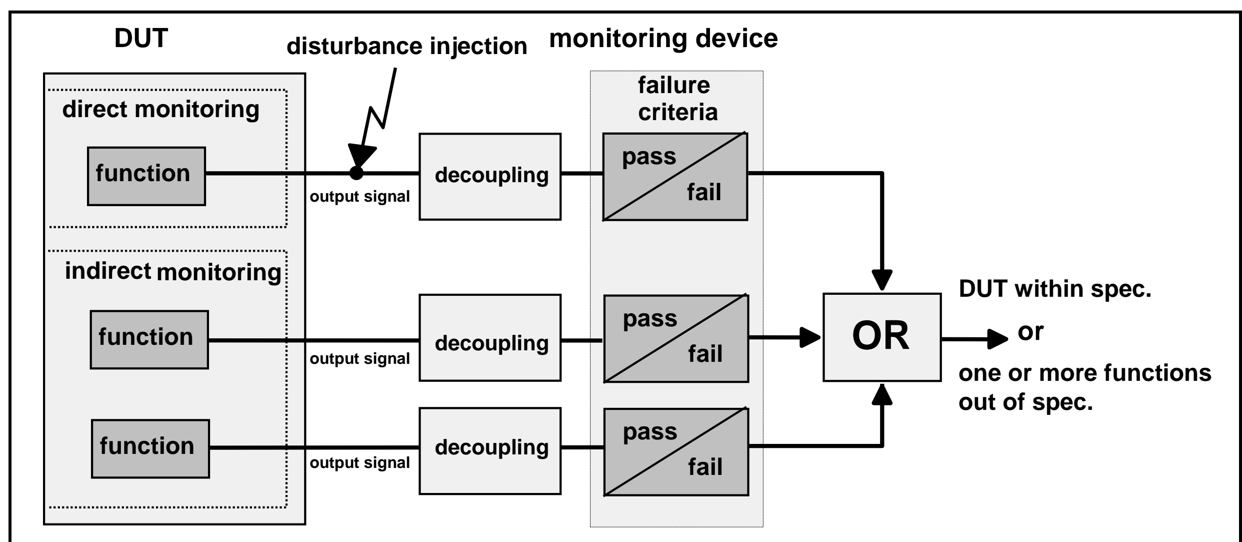


Figure 20: DUT monitoring

Failure criteria:

For monitored signals failure criteria have to be defined in the dedicated IC EMC test specification. A failure criterion is defined by its nominal signal values and allowed tolerances. An example of failure criteria for typical signals is shown in Table 35.

failure criterion no.	monitored function	failure criteria
1	analog output	2,5 V ± 0,2 V
2	'status' output	digital signal '1'
n	…	…

Table 35: Example of a failure criteria table

Disturbance signatures superposed on the monitored signal are not regarded as failure caused by the IC under test and shall not be considered.

Activated protection or diagnosis functions (over voltage, under voltage, over current, etc.) or for example current variations caused by changing operation conditions during transient pulse injection test shall not be regarded as functional failure but have to be noted in the test report.

9.1.3 Monitoring setup

The signal decoupling- and monitoring setup with or without external filter elements should not affect functional signals and not significantly reduce injected disturbance signals. It is recommended that the filter impedance is higher than 400 Ω in the test frequency range. An example of filter definition is shown in Figure 21.

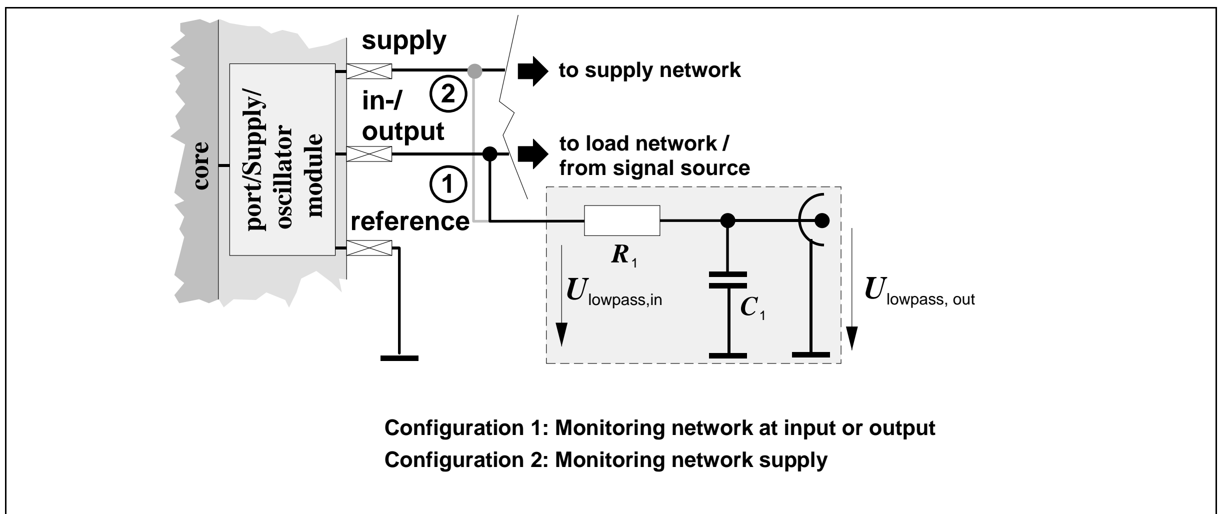


Figure 21: General setup for a decoupling network for monitoring

Basis of filter calculation:

transfer ratio: $$a = \frac{U_{\text{lowpass,out}}}{U_{\text{lowpass,in}}} = \frac{1}{1 + j2\pi f R_1 \cdot C_1}$$

magnitude of the transfer ratio in dB $$|a| = \left|\frac{U_{\text{lowpass,out}}}{U_{\text{lowpass,in}}}\right| = 20 \cdot \log\left\{\frac{1}{\sqrt{1 + 4\pi^2 f^2 R_1^2 C_1^2}}\right\}$$

Limit for the magnitude of the transfer ratio < -20 dB, requires R_1 > 400 Ω in the test frequency range

Note: Reflection coefficient for $R_1 \geq 400\ \Omega$ in a 50 Ω system ≥ 0,8

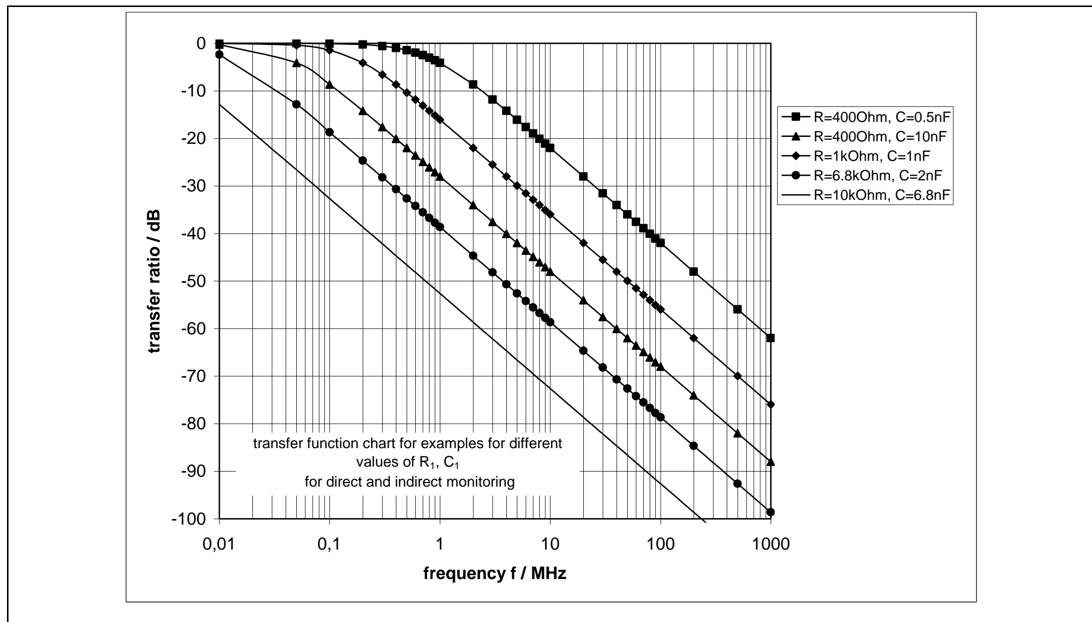


Figure 22: Decoupling network for monitoring: transfer functions for low pass circuitry examples

9.1.4 Performance classes for immunity testing

The *FFU functional states* are defined in [10].

performance class	definition	similar to FPSC in ISO 11452-1
A_{IC}	all monitored functions of the IC perform within the defined tolerances during and after exposure to disturbance	I
B_{IC}*)	short time degradation of one or more monitored signals during exposure to disturbance is not evaluable for IC only. Therefore this classification may not be applicable for ICs	
C_{IC}	at least one of the monitored functions of the IC is out of the defined tolerances during the disturbance but returns automatically to the defined tolerances after exposure to disturbance	II
$D1_{IC}$, $D2_{IC}$	at least one monitored function of the IC does not perform within the defined tolerances during exposure and does not return to normal operation by itself. The IC returns to normal operation by manual intervention class D1: reset class D2: power cycling	 III IV
E_{IC}	at least one monitored function of the IC does not perform within the defined tolerances after exposure and cannot be returned to proper operation	

Table 36: Definition of performance classes

***) Note:** Short time degradation of one or more monitored signals might be tolerable in the application by its error handling. This error handling is unknown in most cases for IC test.

9.2 (G)TEM-cell setup

The measurement of radiated electromagnetic fields with the (G)TEM cell and the immunity against electromagnetic fields with the (G)TEM cell shall be performed according to [2] and [7].

With the (G)TEM cell the field coupling between the IC structure and the (G)TEM cell septum is measured. Therefore the IC is mounted on one side of the test board, which is oriented to the septum of the (G)TEM cell. All other circuit elements are located on the other side of the test board and therefore outside of the (G)TEM cell.

(G)TEM cell measurements shall be performed in at least two orientations with 90° rotation in the *x*- and *y*- direction. The data sets shall be documented separately for each direction.

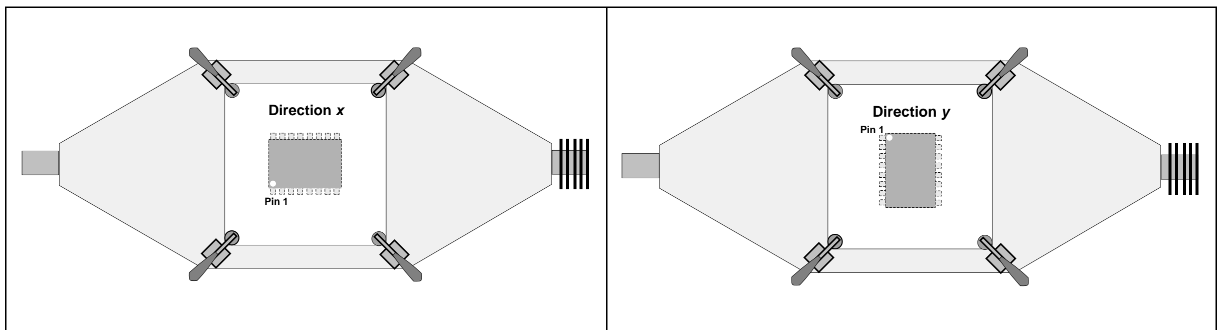


Figure 23: Example of "Direction *x*" and "Direction *y*" of TEM cell test PCB

9.3 IC stripline setup

The measurement of radiated electromagnetic fields with the IC stripline and the immunity against electromagnetic fields with the IC stripline are measured according to [9] and [5].

With the IC stripline the field coupling between the IC structure and the IC stripline septum is measured. The default value for the distance between septum and test board reference ground plane is 6,7 mm. The IC is mounted on one side of the test board, which is oriented to the septum of the IC stripline. All the other circuit elements are located on the other side of the test board.

IC stripline measurements have to be performed for two orientations with 90° difference in the *x*- and *y*- plane at least. The data sets shall be documented separately for each direction.

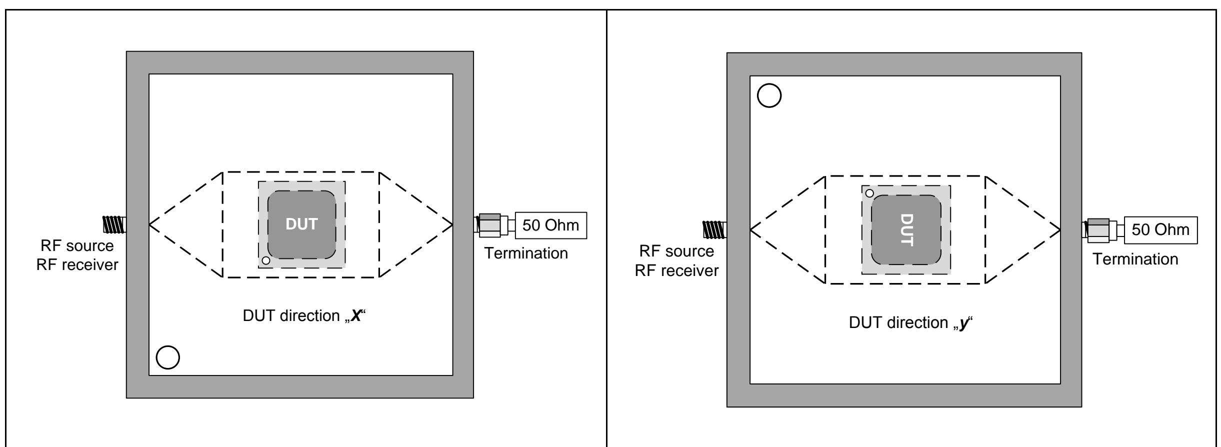


Figure 24: Example of "Direction X" and "Direction Y" of IC stripline test PCB

9.4 System level ESD test setup

The setup for unpowered system level ESD test consisting of test PCB, ESD generator, PCB fixture and GND reference are shown in Figure 25 and Figure 57. The ESD generator return shall be connected to the test PCB GND directly or via the test PCB fixture. For automated test systems the contact discharge tip of the ESD generator can be replaced by an appropriated spring tip.

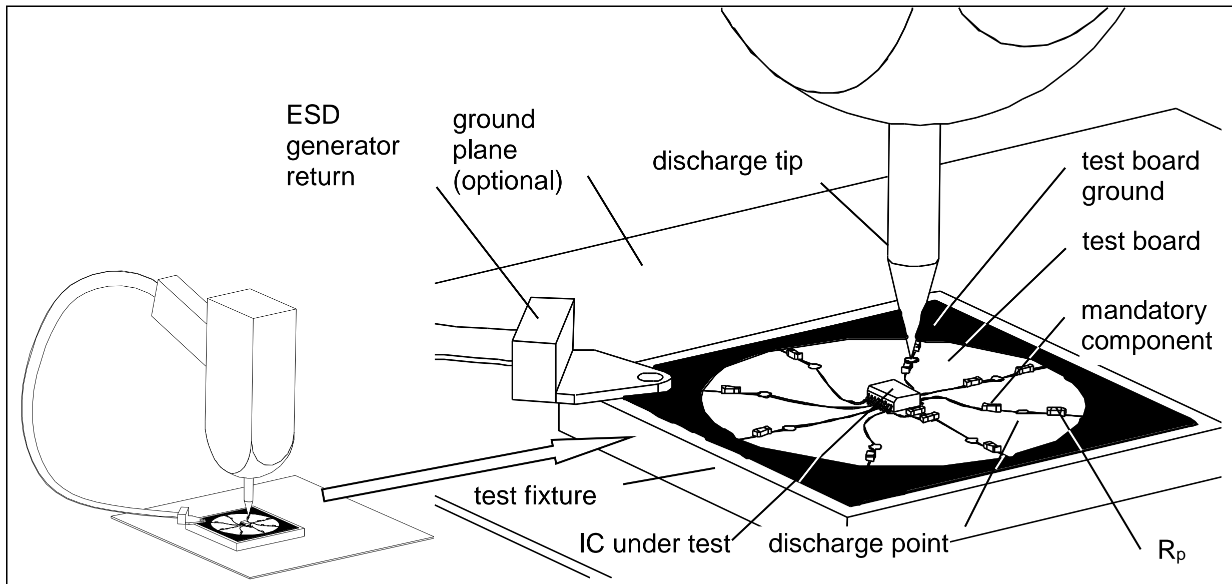


Figure 25: System level ESD test setup

9.5 Test board

9.5.1 General

The minimum requirement for the test PCB is a two-layer board with a common ground plane on the bottom side used as reference ground.

An IC- socket might be used on the test board for transient pulse und system level ESD tests if the applied test signal at the pin has a rise time longer than 5ns (e.g. if any device is between the discharge point and the pin under test which limits the signal rise time).

In general all ground areas should be connected to a common ground system.

9.5.2 RF emission and immunity

For conducted measurements the geometry of the board may have any rectangular or circular shape. This is dependent on the IC specific application and necessary additional components, measuring- and decoupling networks. The DUT and all mandatory components needed to operate the DUT, as described in the data sheet or application note should be mounted onto the topside of the test board. As much wiring as possible should be routed in the top layer. The device under test should be placed in the centre of the PCB, while the needed matching networks should be placed around this centre. The wiring between the IC pins and the matching network should be as short as possible. A trace length equal to 1/20 of the shortest occurring wave length (1 GHz) is a reasonable target. The wiring of the outputs of the matching networks should be designed to have a line impedance of 50 Ω connected with a RF-connector (e.g. SMA or SMB) at the end. If the 1 Ω -Method is used a socket for the RF current probe should be used. The shield of the RF current probe tip shall be connected to RF- peripheral ground by the socket, while the measured IC Pin is connected to the current probe tip. The connection between the

IC Pin and the probe tip should be as short as possible. In any case the trace length should not exceed 15 mm (at 1 GHz upper frequency range limit).

In general the transfer characteristic of each RF measurement point at the test board including all functional, decoupling and measuring components without the DUT shall be measured and documented in the test report. The DUT has to be substituted by 50 Ω resistors to ground at the DUT pin pads.

For radiated RF measurements with (G)TEM-cell or IC stripline the geometry of the board is given by the hole in the (G)TEM cell or IC stripline fixture where the board has to fit in. To fulfill the requirements of the application on such a limited board a multi-layer board should be used. In any case the DUT has to be mounted on the bottom side with the common ground plane.

Examples of board layouts for 150-Ω -, 1-Ω - , DPI- and (G)TEM-cell testing are shown in Annex C.

9.5.3 Transient pulses

For transient pulse tests the RF emission and immunity test board can be reused if the test board is designed to handle the voltage and current characteristics of the applied transient pulses.

9.5.4 System level ESD

For unpowered system level ESD tests a well defined test board shall be used to provide test conditions similar to application conditions for global pins and to achieve high reproducibility of results.

The DUT shall be assembled on top of the test board and all pins under test should be connected directly by a trace to the discharge point without any via to ensure proper test signal transfer to the pin. The length of the discharge trace should be as short as possible (e.g. < 30 mm) and the trace width (e.g. 0,254 mm) shall handle the expected discharge current without significant attenuation. If a directional change of the discharge trace is necessary it shall be designed with rounded corners or an angle < 45°. The Discharge point, where the tip of the ESD generator shall be connected, should have a circular shape with a diameter of e.g. 3 mm and a connected via of 1.5 mm to snap in the discharge tip. Alternatively a landing pad of e.g. 3 mm without via should be designed for connecting the ESD generator by a spring tip to the board. To avoid sparkover between discharge point and reference ground a distance of e.g. > 5 mm should be assured. The bottom side of the test board shall be designed as GND reference plane. The GND connection of the ESD generator to the test board GND can be realized e.g. by a socket, metallic frame or test fixture. If mandatory or additionally recommended components are used they shall be placed close to the DUT. The DUT can also be connected by an IC socket, if the rise time of the test signal is reduced by external components or not affecting the test results.

Examples of test boards are given in Annex C.

10 Functional configurations and operating modes

The functional configuration of the FFUs describes the operation of the sources and sinks in a FFU during the emission measurement or immunity test period. The pin loading is given by the test and measurement networks described in chapter 8. Any deviations of the functional or hardware configuration have to be noted in the test report.

10.1 Test configuration for ICs without CPU

10.1.1 Emission test configuration

port modules	PM1	**line driver** To measure the direct switching noise of a line driver the driver shall operate with the maximum frequency and the shortest switching time as specified in the IC data sheet. The duty cycle should be set to 50 %. If there is a function integrated to use EMC optimized operation modes they should be measured additionally. If more than one driver is tested simultaneously all drivers have to be controlled synchronously. For core cross coupling noise measurement the line driver has to be set in a permanent high state. This measurement should be performed only if a cross coupling by internal periodical sources with frequencies above 1 MHz is expected. LIN communication drivers have to be tested according to EMC evaluation of LIN transceivers [20].
	PM2	**line receiver** To measure the core cross coupling emission at a line receiver the receiver has to be set in the normal receiving mode. This measurement should be performed only if a cross coupling by internal periodical sources with frequencies above 1 MHz is expected. LIN communication receivers have to be tested according to EMC evaluation of LIN transceivers [20].
	PM3	**symmetrical line drivers** To measure the direct switching noise of a symmetrical line driver the drivers shall operate with the maximum frequency and the shortest switching time as specified in the IC data sheet. The duty cycle should be set to 50 %. If there is a function integrated to use EMC optimized operation modes they should be measured additionally. For core cross coupling emission measurement the line driver has to be set in a permanent high state. This measurement should be performed only if a cross coupling by internal periodical sources with frequencies above 1 MHz is expected. CAN symmetrical line drivers have to be tested according to specification EMC evaluation of CAN-Transceivers [19].
	PM4	**symmetrical line receiver** To measure the core cross coupling emission of a symmetrical line receiver the receiver has to be set in the normal receiving mode. This measurement should be performed only if a cross coupling by internal periodical sources with frequencies above 1 MHz is expected. CAN communication receivers have to be tested according to EMC evaluation of CAN transceivers [19].

	PM5	**regional driver** To measure the direct switching noise of a regional driver the driver shall operate with the maximum frequency and the shortest switching time as specified in the IC data sheet. The duty cycle should be set to 50%. If there is a function integrated to use EMC optimized operation modes they should be measured additionally. For core cross coupling noise measurement the regional driver has to be set in a permanent high state to measure effects caused by internal periodical sources. This measurement should be performed only if a cross coupling by internal periodical sources with frequencies above 1 MHz is expected. To measure the pin to pin cross coupling noise caused by the neighbouring pins the measured pin shall be set at high level and the neighbouring pins shall operate with the maximum frequency and the shortest switching time as specified in the IC data sheet. The duty cycle should be set to 50%.
port modules	PM6	**regional input** For core cross coupling noise measurement the regional input shall stay in the default state to measure effects caused by internal periodical sources. This measurement should be performed only if a cross coupling by internal periodical sources with frequencies above 1 MHz is expected.
	PM7	**high side driver** To measure the direct switching noise of a high side driver the driver shall operate with the maximum frequency and the shortest switching time as specified in the IC data sheet. The switching time should take less than 1% of the switching period. The duty cycle should be set to 50%. If there is a function integrated to use EMC optimized operation modes they should be measured additionally with the same frequency as before. For core cross coupling noise measurement the high side driver has to be set in a permanent high state to measure effects caused by internal periodical sources. This measurement should be performed only if a cross coupling by internal periodical sources with frequencies above 1 MHz is expected.
	PM8	**low side driver** To measure the direct switching noise of a low side driver the driver shall operate with the maximum frequency and the shortest switching time as specified in the IC data sheet. The switching time should take less than 1% of the switching period. The duty cycle should be set to 50%. If there is a function integrated to use EMC optimized operation modes they should be measured additionally with the same frequency as before. For core cross coupling noise measurement the low side driver has to be set in a permanent high state to measure effects caused by internal periodical sources. This measurement should be performed only if a cross coupling by internal periodical sources with frequencies above 1 MHz is expected.
supply module	SM1	To measure the emission on the supply the IC shall be powered as for normal operation. All modules shall operate as defined for normal operation according to data sheet. All internal periodical sources shall be active and operate with maximum frequency and power.
core module	CM1	The core module shall operate as defined for normal IC function. All internal periodical sources shall be active and operate with maximum frequency and power.
oscillator module	OM1	If an oscillator is used it has to be activated and operate with maximum frequency and power as specified.

Table 37: Emission test configuration for ICs without CPU

10.1.2 Immunity and transient test configuration

port modules	PM9	**line driver** To measure the immunity of a line driver two functional operation modes have to be tested. In the first mode the driver shall operate with a typical frequency and the typical switching time as specified in the IC data sheet. The duty cycle should be set to 50%. In the second mode the driver has to be set in a permanent high state. For both operation modes the functionality shall be monitored directly at the line driver pin and indirectly at another functional module output port of the IC to detect cross coupling effects to other FFUs. If there is a function integrated to use EMC optimized operation modes they should be measured additionally. If more than one driver is tested simultaneously all drivers have to be controlled synchronously. LIN communication drivers have to be tested according to EMC evaluation of LIN transceivers [20].
	PM10	**line receiver** To measure the immunity at a line receiver the receiver has to be set in the normal receiving mode. The monitoring shall be done indirectly at another FFU functional module output port of the IC to detect cross coupling effects to other FFUs. There is no possibility to distinguish between the immunity behavior of the receiver and cross coupling effects into other FFUs. LIN communication receivers have to be tested according to EMC evaluation of LIN transceivers [20].
	PM11	**symmetrical line driver** To measure the immunity of a symmetrical line driver two functional operation modes have to be tested. In the first mode the driver shall operate with a typical frequency and the typical switching time as specified in the IC data sheet. The duty cycle should be set to 50%. In the second mode the driver shall be deactivated and stay in the default state. For both operation modes the functionality shall be monitored directly at the line driver pin and indirectly at another functional module output port of the IC to detect cross coupling effects to other FFUs. If there is a function integrated to use EMC optimized operation modes they should be measured additionally. CAN communication drivers have to be tested according to EMC evaluation of CAN transceivers [19].
	PM12	**symmetrical line receiver** To measure the immunity of a symmetrical line receiver the receiver has to be set in an active receiving mode. The monitoring shall be done indirectly at another functional module output port of the IC to detect cross coupling effects to other FFUs. There is no possibility to distinguish between the immunity behavior of the receiver and cross coupling effects into other FFUs. CAN communication receivers have to be tested according to EMC evaluation of CAN transceivers [19].
	PM13	**regional driver** To measure the immunity of a regional driver three functional operation modes are possible. The test shall be performed at least in the toggling mode with a typical frequency and the typical switching time as specified in the IC data sheet. The duty cycle should be set to 50%. Optionally the driver can be tested in a permanent high state and/or low state. For all operation modes the functionality shall be monitored directly at the regional driver pin and indirectly at another functional module output port of the IC to detect cross coupling effects to other FFUs. If there is an integrated function for EMC optimized operation modes these should be tested additionally.

<table>
<tr><td rowspan="3">port modules</td><td>PM14</td><td>regional input
To measure the immunity of a regional input the input has to be set in an active mode.
The monitoring shall be done indirectly at another functional module output port of the IC to detect cross coupling effects to other FFUs. There is no possibility to distinguish between the immunity behaviour of the input and cross coupling effects into other FFUs.</td></tr>
<tr><td>PM15</td><td>high side driver
To measure the immunity of a high side driver three functional operation modes are possible. The test shall be performed at least in the toggling mode with a typical frequency and the typical switching time as specified in the IC data sheet. The duty cycle should be set to 50%. Optionally the driver can be tested in a permanent high state and/or low state.
For all operation modes the functionality shall be monitored directly at the high side driver pin and indirectly at another functional module output port of the IC to detect cross coupling effects to other FFUs.
If there is an integrated function for EMC optimized operation modes these should be tested additionally.</td></tr>
<tr><td>PM16</td><td>low side driver
To measure the immunity of a Low Side driver three functional operation modes are possible. The test shall be performed at least in the toggling mode with a typical frequency and the typical switching time as specified in the IC data sheet. The duty cycle should be set to 50%. Optionally the driver can be tested in a permanent high state and/or low state.
For all operation modes the functionality shall be monitored directly at the Low Side driver pin and indirectly at another functional module output port of the IC to detect cross coupling effects to other FFUs.
If there is an integrated function for EMC optimized operation modes these should be tested additionally.</td></tr>
<tr><td>supply module</td><td>SM2</td><td>To measure the immunity of the supply the IC shall be powered for normal operation. All modules shall operate as defined for normal operation according to data sheet. All internal periodical sources shall be active and operate with maximum frequency and power.
The monitoring shall be done indirectly at the supplied FFUs of the IC.</td></tr>
<tr><td rowspan="2">core module</td><td>CM2</td><td>core active mode
The core module shall operate as defined for normal IC function. All internal functions shall be active and operate with typical frequency and power.</td></tr>
<tr><td>CM3</td><td>core sleep modes
If it is possible to set the IC in other modes different to the normal mode such as sleep mode, standby mode etc. these should be tested additionally.</td></tr>
<tr><td>oscillator module</td><td>OM2</td><td>If an oscillator is used it has to be activated and operate with typical frequency and power as specified.</td></tr>
</table>

Table 38: Immunity test configuration for ICs without CPU

10.2 Test configuration for ICs with CPU

10.2.1 Software initialization for emission tests

<table>
<tr><th colspan="4">configuration software module</th><th rowspan="2">description and definition of test <u>initialization</u> software module</th></tr>
<tr><th>number</th><th colspan="2">name</th><th>short description</th></tr>
<tr><td>C1</td><td colspan="2">reference</td><td>'worst case' setting</td><td>system clock: - frequency $f = f_{max}$
CPU: - active
FFUs: - all Fixed-function Units active, if available: system clock output active
active ports: - all multifunction ports switched to FFU function
- fastest slew rate of drivers
inactive Ports: - all other ports
memory access: - choose the memory access for the loop software module with highest emission potential available, for example:
- synchronous access from external memory (burst mode)
- asynchronous access from external memory
- internal access from on-chip memory</td></tr>
<tr><td>C2</td><td rowspan="2">bus mode</td><td>1</td><td>program execution with synchronous bus access/ system clock</td><td>system clock: - frequency $f = f_{max}$
CPU: - active
FFUs: - all Fixed-function Units inactive, except the memory interface
active ports: - buses
- bus clock (system clock output active)
- fastest slew rate of drivers
inactive Ports: - all other ports
memory access: - memory access for the loop software module: synchronous access from external memory (burst mode)</td></tr>
<tr><td>C3</td><td>2</td><td>program execution with asynchronous bus access/ system clock</td><td>system clock: - frequency $f = f_{max}$
CPU: - active
FFUs: - all Fixed-function Units inactive, except the memory interface
active ports: - buses
- fastest slew rate of drivers
inactive Ports: - all other ports
- bus clock (System clock output inactive)
memory access: - memory access for the loop software module: asynchronous access from external memory</td></tr>
</table>

C4	bus mode 3	on-chip execution without system clock output	system clock:	- frequency $f = f_{max}$
			CPU:	- active
			FFUs:	- all *Fixed-function Units* inactive
			active ports:	- none
			inactive Ports:	- all ports (Buses and all other ports) - bus clock (System clock output inactive)
			memory access:	- memory access for the loop software module: internal access from on-chip memory
C5	driver	driver slew rate test	system clock:	- frequency $f = f_{max}$
			CPU:	- active
			FFUs:	- all *Fixed-function Units* inactive, except the FFU corresponding to a tested driver (if system clock output is available, its test is required)
			active ports:	driver slew rate switched to I. Required: fastest slew rate II. Optional: slower slew rates
			inactive ports:	- all other ports
			memory access:	choose the memory access for the loop software module with lowest emission potential (*low, medium, high*) available, for example: *low* internal access from on-chip memory *medium* asynchronous access from external memory *high* synchronous access from external memory (burst mode)
C6	oscillator	idle (Oscillator) mode	system clock:	- frequency = f_{max}
			CPU:	- inactive ('wait' mode, 'hold' mode), if available
			FFUs:	- all Fixed-function Units functionally inactive and unclocked
			active ports:	- none
			inactive Ports:	- all ports
			memory access:	- memory access for the loop software module: none
C7	clock tree	active clock tree mode	system clock:	- frequency $f = f_{max}$ - maximum clock tree frequency in clock tree distribution
			CPU:	- inactive ('wait' mode, 'hold' mode), if available
			FFUs:	- all Fixed-function Units clocked, but functionally inactive
			active ports:	- none
			inactive Ports:	- all ports
			memory access:	- memory access for the loop software module: none

C8	single FFU	test single FFU	system clock:	- frequency $f = f_{max}$
			CPU:	- minimum required activity
			FFUs:	- all Fixed-function Units inactive, except the FFU under investigation
			active ports:	- controlled ports by FFU under investigation
			inactive Ports:	- all other ports
			memory access:	choose the memory access for the loop software module with lowest emission potential (low, medium, high) available, for example: low: internal access from on-chip memory medium: asynchronous access from external memory high: synchronous access from external memory (burst mode)
C9	reduced system frequency	on-chip execution at reduced system frequency	system clock:	- frequency $f < f_{max}$
				combined with configuration modules C1..C8

Table 39: Test initialization software module for cores containing a CPU

Notes:
1. The measurement should start after finishing the initialization
2. This table may be extended by further tests agreed between the customer and IC supplier

10.2.2 Software initialization for immunity and transient voltage tests

configuration software module			description and definition of test <u>initialization</u> software module
number	**name**	**short description**	
C10	immunity reference	functional 'Worst case' setting	system clock: - frequency $f = f_{max}$ CPU: - active FFUs: - all *Fixed-function Units* active, *if available:* system clock output active active ports: - all multifunction ports switched to FFU function - fastest slew rate of drivers inactive ports: - all other ports monitor pin: - a pin of a non-multifunction port without FFU function, toggle signal with fixed relation to system clock (constant frequency), CPU-driven error detection: - all possible error detections should be active (e.g. watchdog, oscillator loss of lock, internal/external bus errors / FFU-errors, traps, interrupts) - load/compare/store loop inside internal/external memory - each error case should stop the toggling signal on the monitor pin memory access: choose the memory access for the loop software module with highest functional potential (*high, medium, low*) available, for example: *high* synchronous access from external memory (burst mode) *medium* asynchronous access from external memory *low* internal access from on-chip memory
C11	oscillator	idle mode (oscillator test-mode)	system clock: - frequency $f = f_{oscillator}$ CPU: - inactive ('wait' mode, 'hold' mode), if available FFUs: - all *Fixed-function Units* functionally inactive and unclocked OSC: - all different Oscillator-driver-settings must be tested on a typical crystal (e.g. according to data sheet like 4 MHz / 16 MHz) active ports: - clock output or a toggling port for monitoring inactive Ports: - all ports memory access: - memory access for the loop software module: none

Table 40: Immunity test configuration for ICs with CPU

Notes:
1. The measurement shall start after finishing the initialization
2. This table may be extended by further tests agreed between the customer and IC supplier

10.2.3 Software loop

The software loop is applicable for emission, immunity and transient test.

The test software should be developed with respect to the expected dwell or measurement time.

loop software module		description and definition of test loop software module
number	**short description**	
S0	idle	none
S1	fastest instruction loop	example: label: jump(unconditional) label
S2	RAM copy	Copied data range is equal or more than 10% of available RAM. Data pattern is alternating $AA.. and $55.. (length depending on data bus width) in consecutive RAM access. Source memory area and destination memory area shall differ by the maximum number of address bits memory address vector +1 increment 0xD0000000 AAAAAAAA 0xD0000010 55555555 0xD0000020 AAAAAAAA 10% lower RAM memory area ... 10% upper RAM memory area 0xD001FFE0 55555555 0xD001FFF0 AAAAAAAA 0xD0020000 55555555 memory address vector -1 decrement
S3	driver output action	toggling driver outputs
S4	IEC increment	[IEC 61967-1, annex B]: "This simple routine implements a counter function using a single 8-bit port. Every 100 µs, the port output is incremented or decremented. After 10 count cycles (256 ms) an LED output is complemented. This will provide a blinking light indication with a frequency of about 2 Hz. For consistency, equivalent loop times shall be maintained."
S5	FFU dedicated software	CPU runs at minimum required activity for FFU controlling, target is autonomous running mode of the FFU under investigation All FFU parameters: Adjust to EMC worst case condition
S6	read receiver/input	read receiver/input register

Table 41: Test loop software module for cores containing a CPU

11 EMC limits for automotive ICs

All relevant pins of an IC shall be classified according to the limits given in the following chapters. Mandatory components are regarded as part of the IC and shall be added for the test.

The limit classes are different depending on the requirements given by the application. The application EMC effort is defined by the application itself, ECU housing, number of layers, filters elements etc.

limit class	description
I	low EMC requirement
II	medium EMC requirement
III	high EMC requirement
C	customer specific

Table 42: EMC limits for automotive ICs

11.1 RF emission

11.1.1 Emission level scheme

The following level scheme can be used to classify the emission of ICs.

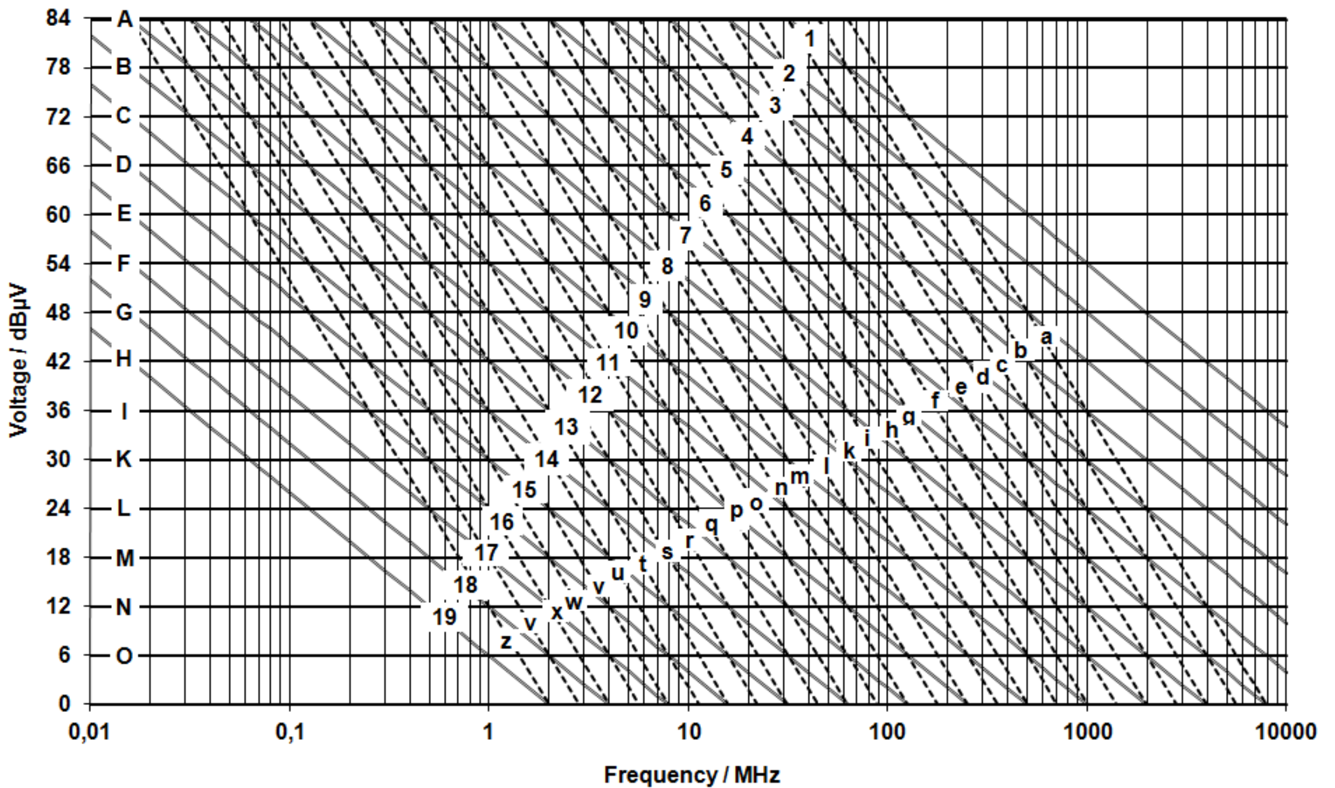


Figure 26: Emission level scheme according to IEC61967-2, IEC61967-4 and IEC61967-8

By selecting the right emission level and defining a limit class for a dedicated IC pin the desired functionality and operation mode has to be considered.

Toggling digital data pins, periodically switching analog power outputs etc. generate switching harmonics as a matter of principle. This may violate emission requirements in terms of standard limit classes but cannot be avoided by IC design measures for functional reasons. The resulting spectrum can be obtained by Fourier transformation of the functional specified signal waveform as described in Annex G. This spectrum describes the limitation of the minimal emission and has to be considered to define superimposed specific limits for those pins.

11.1.2 General emission limit classes

limit class	150 Ω method		1 Ω method		(G)TEM cell method	IC stripline method
	global	local	global	local		
I	8-H	6-F	10-K	8-H	I	F
II	10-K	8-H	12-M	10-K	L	H
III	12-M	10-K	14-O	12-M	N	K
C	customer specific					

Table 43: General emission limit classes

Note: Stripline limits are calculated for stripline with septum height of 6,7 mm (16,6 dB) and adapted to the emission level scheme in Figure 26.

A conversion factor (X) to correlate measuring results of IC striplines with different heights to the default IC stripline height of 6,7 mm can be obtained by:

$$X = 20 * \log\left(\frac{h_1}{h_2}\right)$$

X = conversion factor in dB to IC stripline 6,7 mm height type results
h_1 = active conductor height of specific type
h_2 = active conductor height of 6,7 mm type

conducted emission 150 Ω method limit line set for all IC function modules

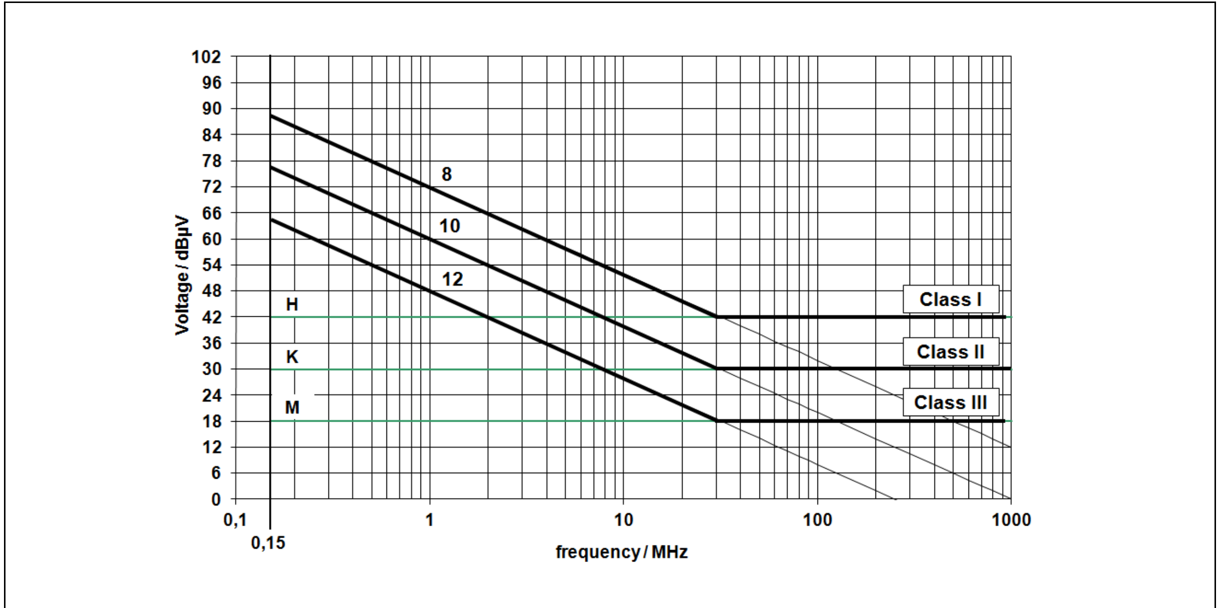


Figure 27: Limit line set 150 Ω method for global pins

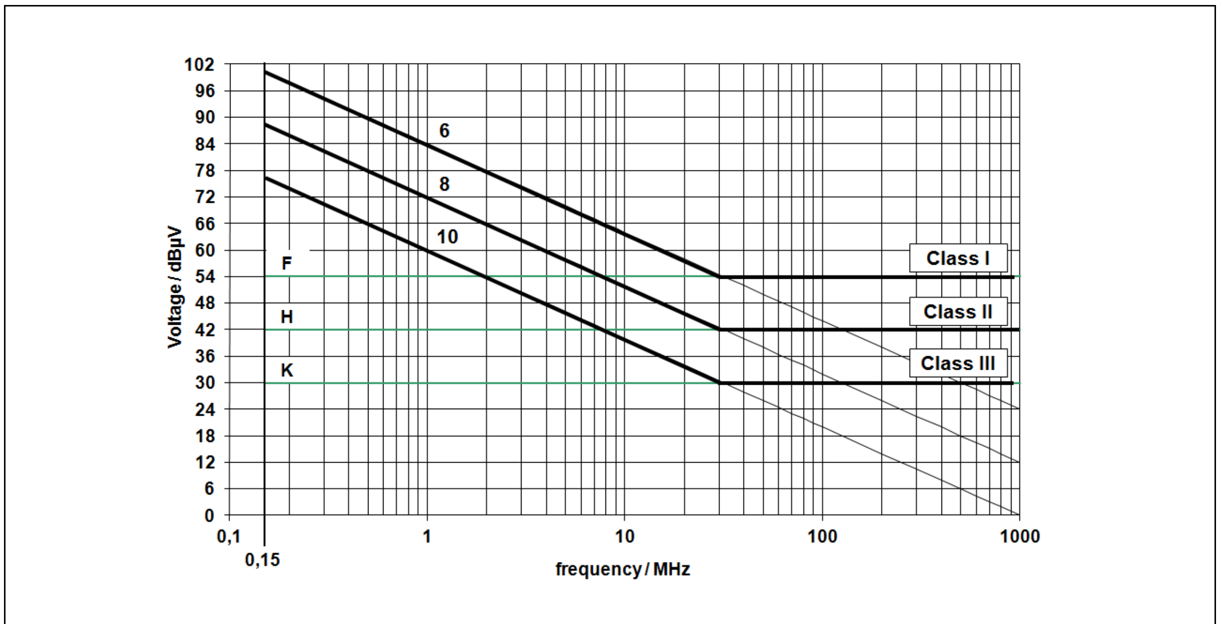


Figure 28: Limit line set 150 Ω method for local pins

conducted emission 1 Ω method limit line set for all IC function modules

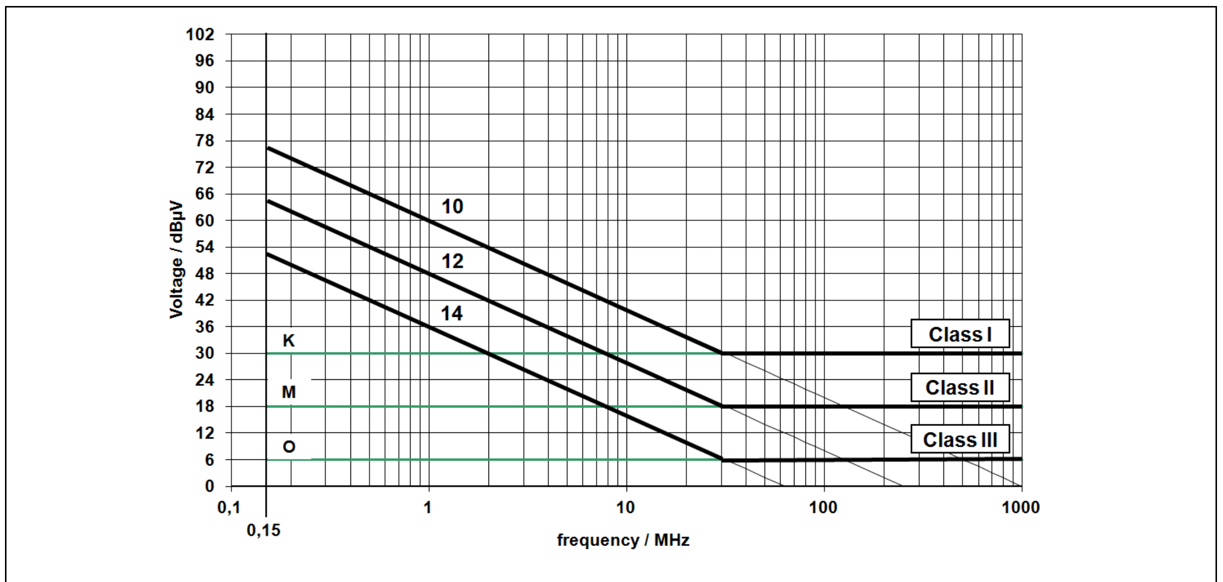


Figure 29: Limit line set 1 Ω emission test method for global pins

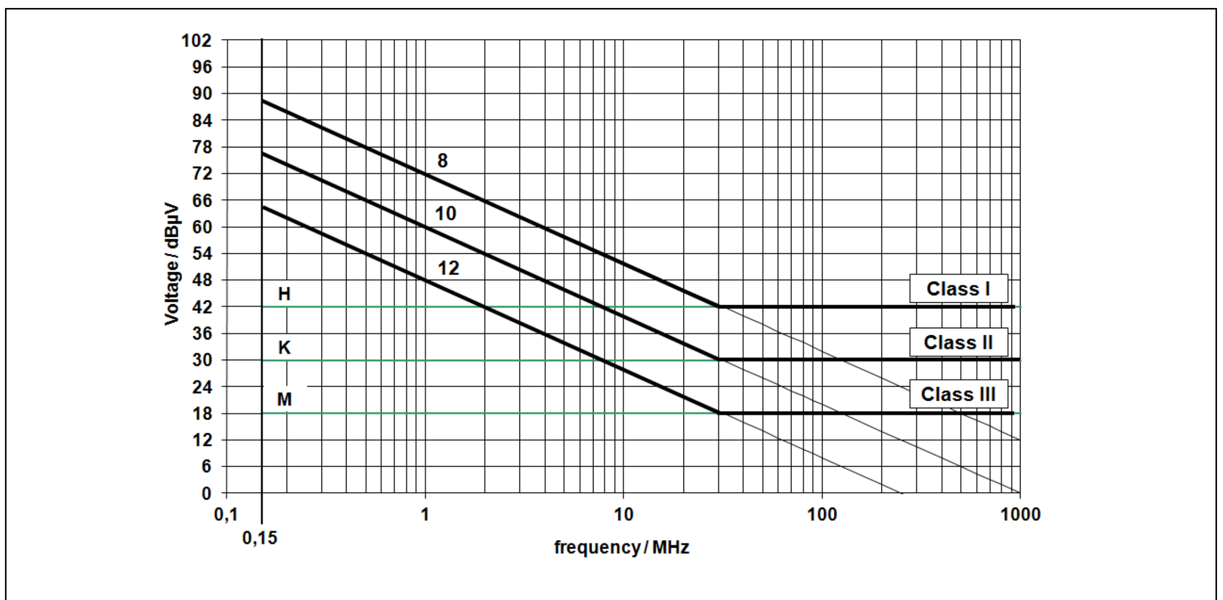


Figure 30: Limit line set 1 Ω emission test method for local pins

radiated emission test methods (G)TEM-cell and IC stripline

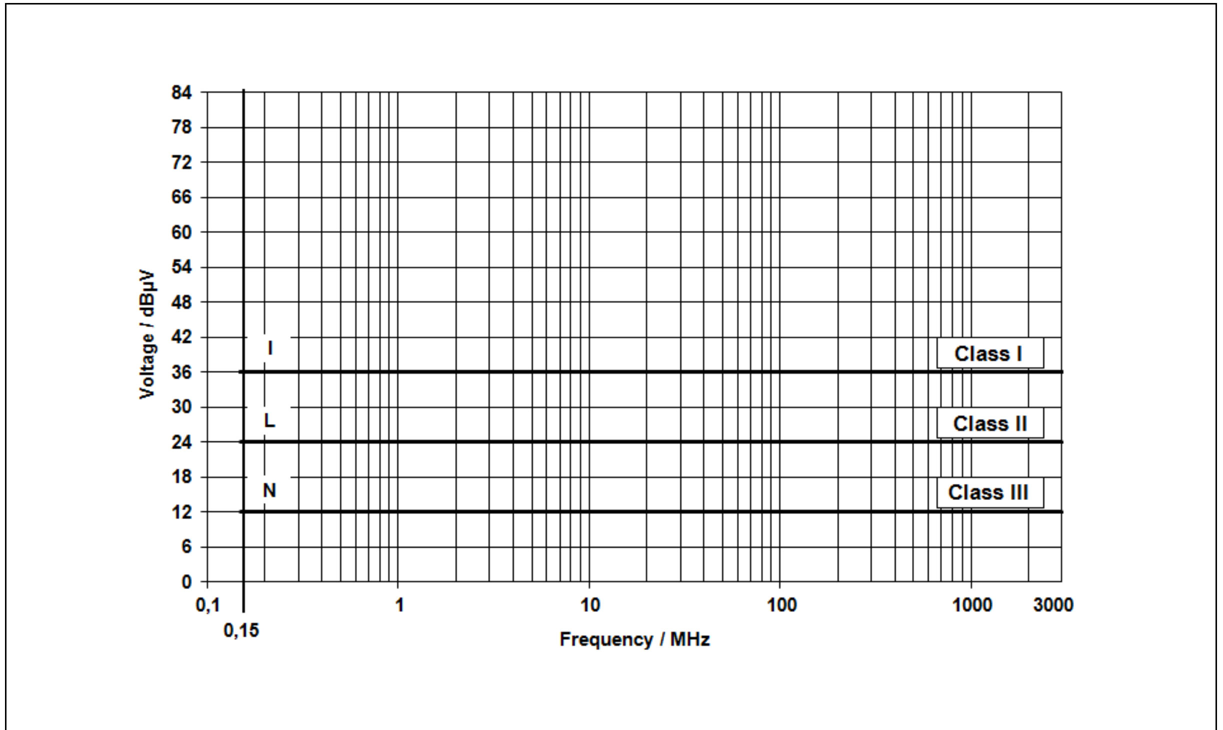


Figure 31: Limit line set for (G)TEM cell emission test method

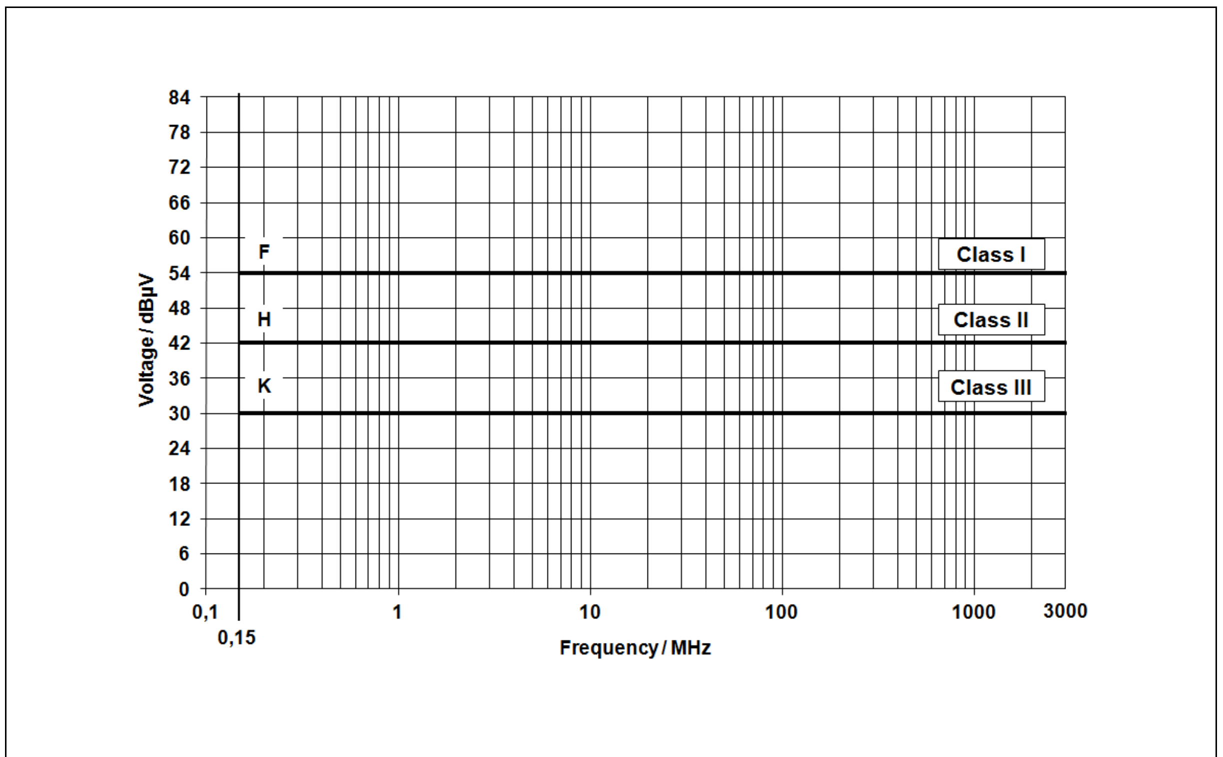


Figure 32: Limit line set for IC stripline emission test method

11.1.3 Emission limits for microcontrollers with external digital bus systems

Adapted limits C-BS for bus communication of microcontrollers with RAM or flash in configuration C1 and software loop S2.

Note: The performance of current 'digital systems' built of ICs of the type microcontroller RAM or flash, connected via busses, leads to higher emission values. To accommodate to this technical phenomenon, other emission values are allowed for this kind of IC type combination. In the case of applying such an IC type combination in an application, all other IC types used in the same application shall fulfil the limit of the agreed region.

emission limits for microcontrollers with external digital bus systems

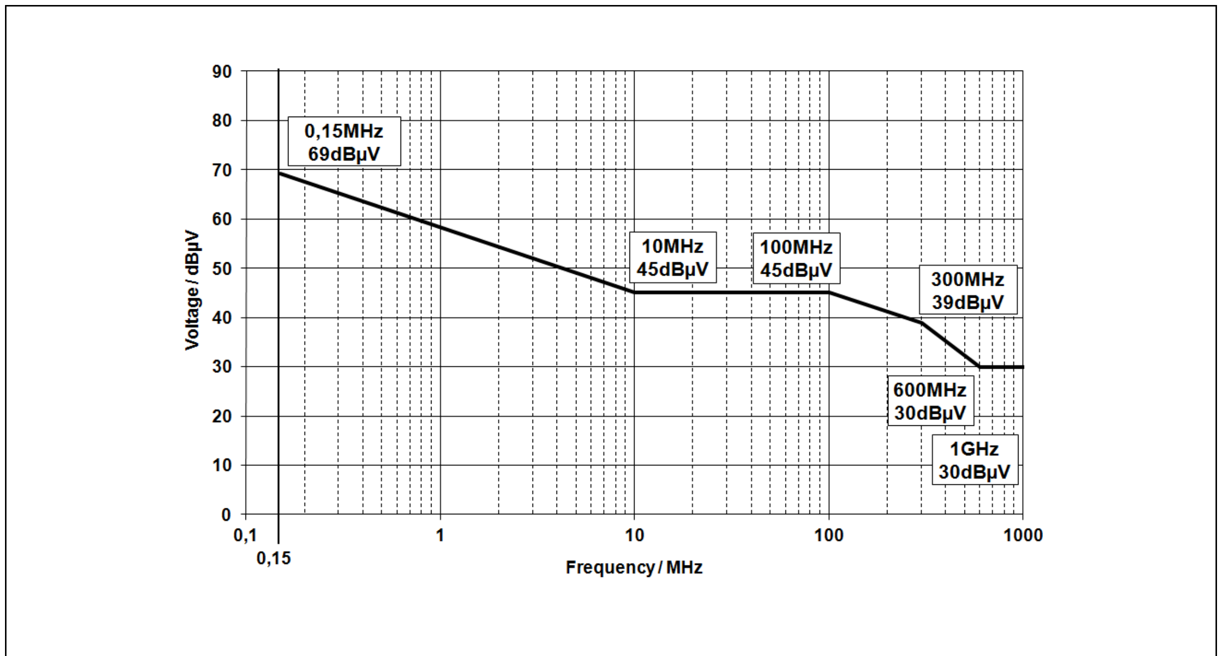


Figure 33: Limit line 150 Ω for port pins of microcontrollers with external digital bus systems

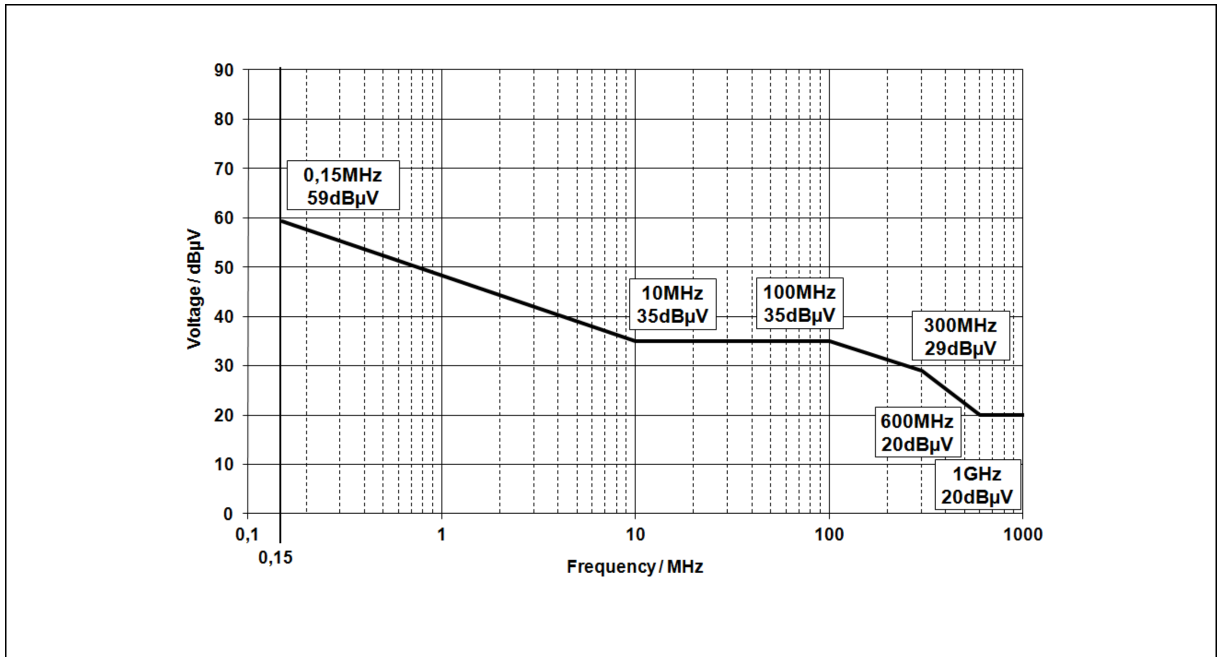


Figure 34: Limit line 150 Ω for supply pins of microcontrollers with external digital bus systems

emission limits for microcontrollers with external digital bus systems

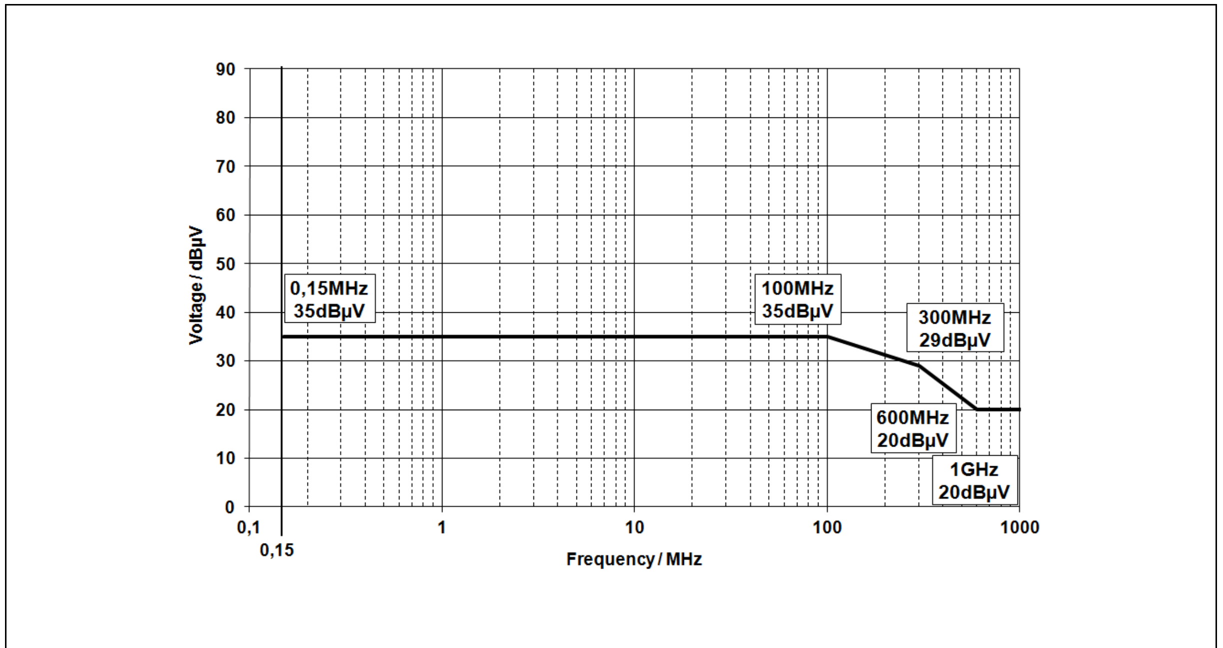


Figure 35: (G)TEM cell limit for microcontrollers with external digital bus systems

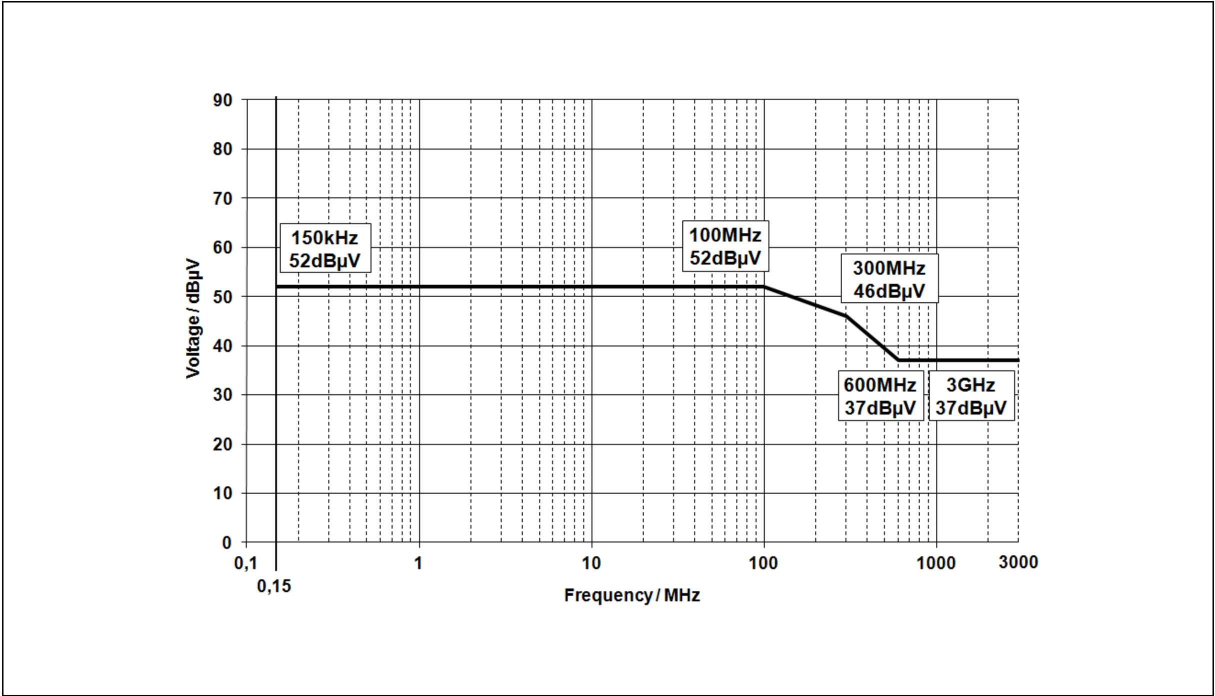


Figure 36: IC Stripline (6,7 mm) limit for microcontrollers with external digital bus systems

11.2 RF immunity

11.2.1 General immunity limit classes

immunity limit classes	DPI forward power / dBm		(G)TEM E-field / (V/m)	IC stripline E-field / (V/m)
	global pin	local pin	entire IC	entire IC
I	18	0	200	200
II	24	6	400	400
III	30	12	800	800
C	customer specific			

Table 44: General immunity limit classes

conducted immunity DPI method limit line set for all IC function modules

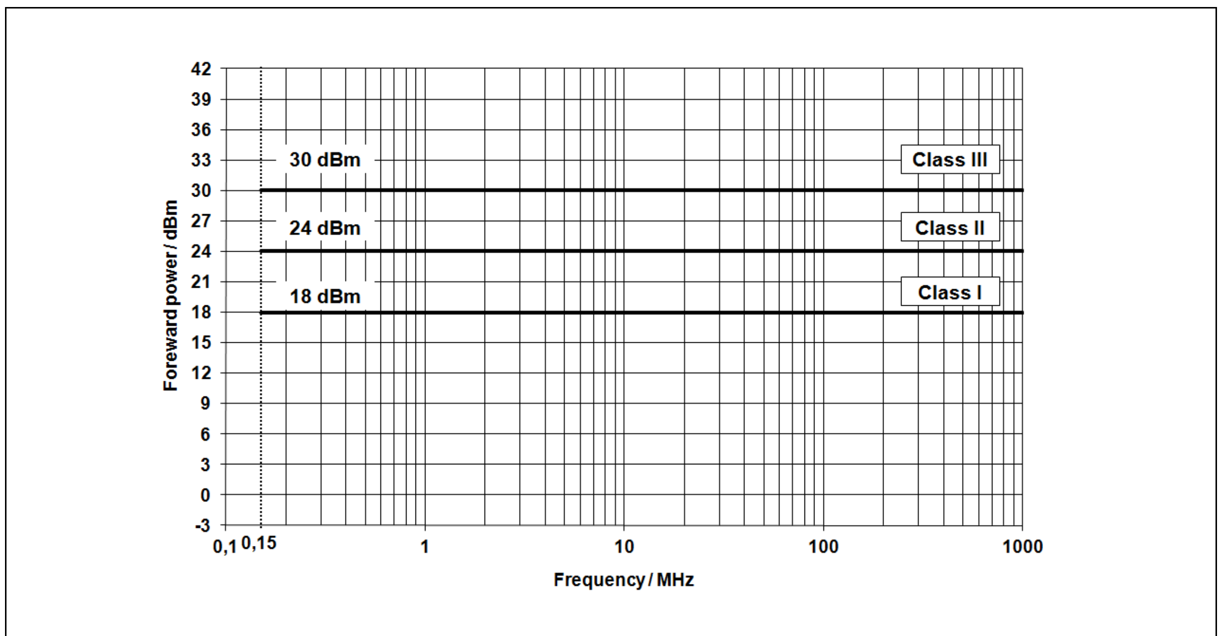


Figure 37: DPI limit line set for global pins

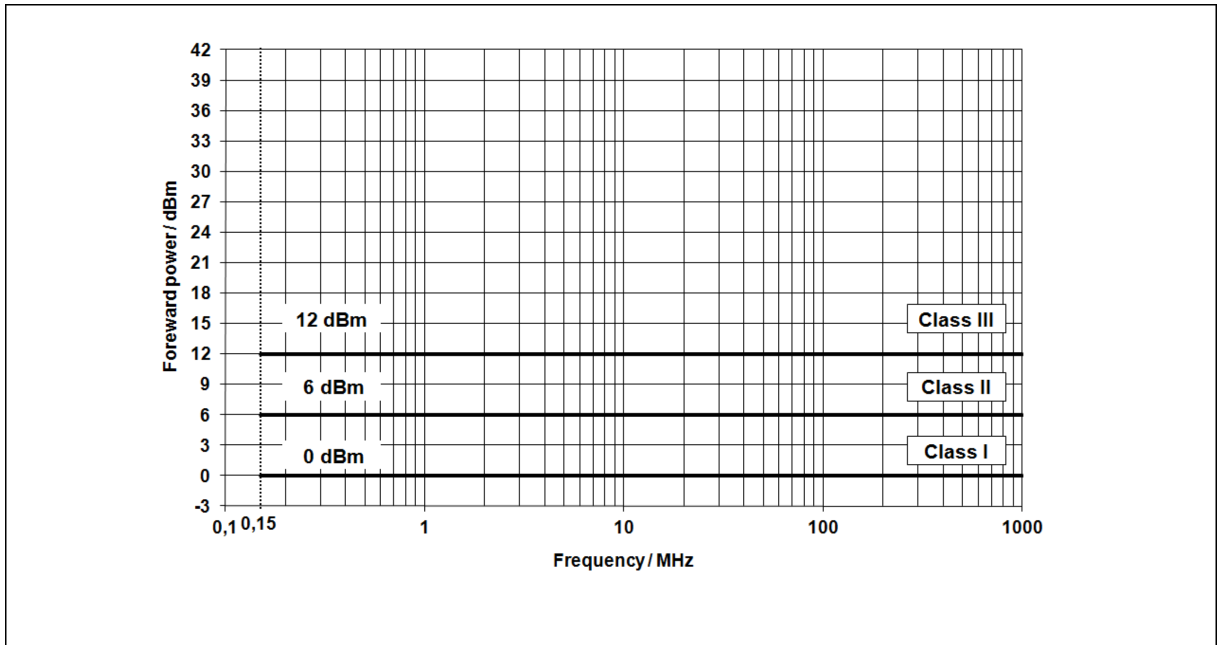


Figure 38: DPI limit line set for local pins

radiated immunity test methods (G)TEM-cell and IC stripline

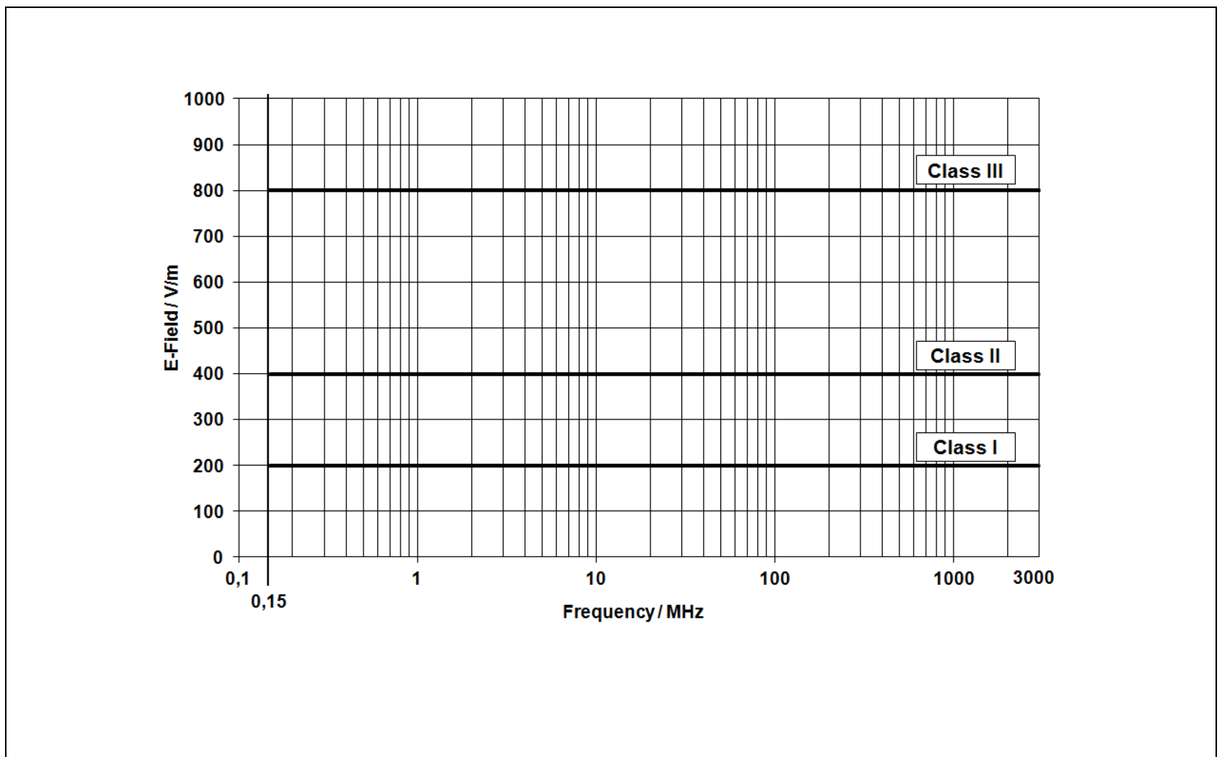


Figure 39: Limit line set for (G)TEM and IC stripline radiated immunity test method

11.3 Pulse immunity

The specified test pulse voltage has to be applied to the pulse injection point. Depending on maximum ratings external protection might be required and test relevance has to be considered.

11.3.1 Preliminary pulse immunity limit classes 12 V

pulse	**immunity limit classes**	**transient exposure pin category / coupling**					**performance class**
		global				**local**	
		1	**2**	**3**	**4**	**5**	
		direct	1nF	direct filtered	1nF filtered	10pF	
ISO 1	I II III	-75 V -112 V -150 V	n/a	-75 V -112 V -150 V	n/a	n/a	C_{IC}
ISO 2a	I II III	37 V 55 V 112 V	n/a	37 V 55 V 112 V	n/a	n/a	A_{IC}, C_{IC}
ISO 3a	I II III	-112 V -165 V -220 V	-112 V -165 V -220 V	-112 V -165 V -220 V	-112 V -165 V -220 V	-112 V -165 V -220 V	A_{IC}, C_{IC}
ISO 3b	I II III	75 V 112 V 150 V	75 V 112 V 150 V	75 V 112 V 150 V	75 V 112 V 150 V	75 V 112 V 150 V	A_{IC}, C_{IC}

Table 45: General immunity limit classes 12V

11.3.2 Preliminary pulse immunity limit classes 24V

pulse	**immunity limit classes**	**transient exposure pin category / coupling**					**performance class**
		global				**local**	
		1	**2**	**3**	**4**	**5**	
		direct	1nF	direct filtered	1nF filtered	10pF	
ISO 1	I II III	-300 V -450 V -600 V	n/a	-300 V -450 V -600 V	n/a	n/a	C_{IC}
ISO 2a	I II III	37 V 55 V 112 V	n/a	37 V 55 V 112 V	n/a	n/a	A_{IC}, C_{IC}
ISO 3a	I II III	-150 V -220 V -300 V	-150 V -220 V -300 V	-150 V -220 V -300 V	-150 V -220 V -300 V	-150 V -220 V -300 V	A_{IC}, C_{IC}
ISO 3b	I II III	150 V 220 V 300 V	150 V 220 V 300 V	150 V 220 V 300 V	150 V 220 V 300 V	150 V 220 V 300 V	A_{IC}, C_{IC}

Table 46: General immunity limit classes 24V

11.4 System level ESD

11.4.1 Preliminary limits for unpowered system level ESD test

pin type	model	ESD generator discharge network		standard	ESD class	ESD level
		C	*R*			
global pin	HBM (system level)	150 pF	330 Ω	ISO 10605 2nd Ed.	I II III C	2 kV 4 kV 6 kV customer specific

Table 47: Preliminary limit classes for unpowered system level ESD tests

12 IC EMC specification

The IC EMC specification for a dedicated IC is either provided by the customer or by the IC supplier. It contains the pin selection, functional configuration, measurement method and limits (EMC requirements) for emission and immunity tests. Additionally the test board's schematic and special agreements may be included. Examples are given in Annex F.

13 Test report

Following items shall be part of the test report:

- References to used specifications and standards
- Schematic diagram of test board
- Pictures of test board layout and/or parts of it
- Description of external components
- Transfer characteristics of RF coupling paths
- Functional configurations of FFUs and description of implemented software modules for ICs with CPU
- Description of test equipment
- Description of monitoring points and failure criteria for immunity and transient voltage tests
- Description of any deviation from previously defined test parameters
- Result diagrams (emission: scaled in dBµV, immunity: scaled in dBm for DPI or V/m for (G)TEM and IC stripline) including limit lines
- Result table for transient and system level ESD tests

14 Contacts and authors

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Table 48: List of contact persons

This specification version 2.1 was created by a working group with experts and members of the German national standardization organization DKE from Bosch, Infineon and Continental. The authors are listed in alphabetical order by companies:

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Dr. Frank Klotz, Thomas Steinecke, Markus Unger

Continental Automotive GmbH:
Felix Müller, Christian Rödig, Gerhard Schmid

Other authors, listed in alphabetical order, have contributed to a previous version of this specification: Dr. Jörg Brückner, Michael Jöster, Herman Roozenbeek, Andreas Rupp, Christoph Schulz-Linkholt.

Annex A
Test network modification
(emission, normative)

A.1 Start frequency calculation

The following hints help to calculate new start frequencies in case of modified coupling capacitors of the 150-Ω-measuring network.
Basis of calculation:

transfer ratio highpass voltage divider $a = \frac{U_{\text{highpass,out}}}{U_{\text{highpass,in}}} = \frac{Z_{\text{in}}}{Z_{\text{out}}}$; limit definition $a\big|_{-3\text{dB}} = \frac{1}{\sqrt{2}}$ (A1)

Magnitude of transfer ratio of 150 Ω network, see Figure 40.

$$|a| = \left|\frac{U_{highpass,out}}{U_{highpass,in}}\right| = 20 \cdot \log \left| \frac{(51\,\Omega \| 50\,\Omega)}{\sqrt{(120\,\Omega + 51\,\Omega \| 50\,\Omega)^2 + \frac{1}{4\pi^2 f^2 C^2}}} \right|$$

transfer ratio for $f \to \infty$: $|a_{f\to\infty}| = 15{,}2$ dB (A2)

Equation for limit frequency (highpass -3 dB point): $f_{-3dB}\big|_{MHz} \approx \frac{1}{844\,\Omega \cdot C\big|_{\mu F}}$ (A3)

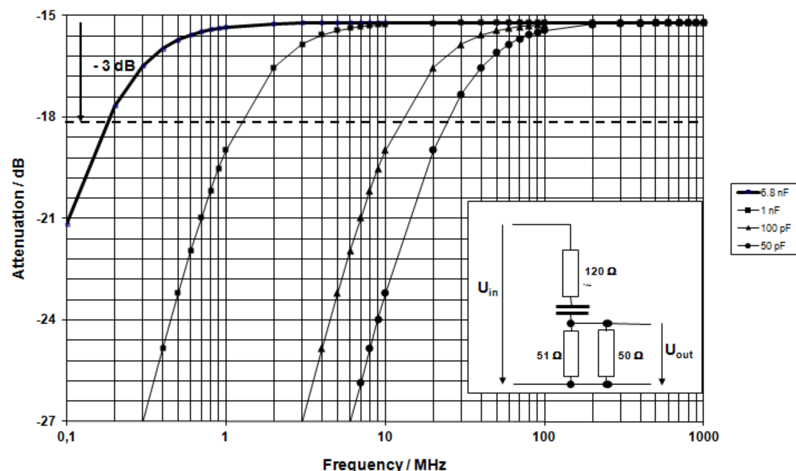

Figure 40: 150 Ω network, attenuation chart of some example capacitor values

Table of useful capacitor values:

value of 150 Ω network DC block capacitor	lower limit frequency (-3 dB)
100 nF	11 kHz
6,8 nF *)	174 kHz
1 nF	1,2 MHz
100 pF	12 MHz
68 pF	17 MHz
50 pF	24 MHz
33 pF	36 MHz

Table 49: Limit frequencies of modified DC block capacitor values in 150 Ω network
***) Note:** Default value according to IEC standard

Annex B
Test definition for ICs with RF antenna pins
(normative)

B.1 General

RF antenna pins cannot be tested with conducted IC EMC test methods as defined in [3, 8]. The only exception would be a conducted emission measurement in a 50 Ω system at a 50 Ω matched network directly connected to the RF measuring receiver for information purpose.

Furthermore ICs with RF antenna pins cannot be tested properly with radiated IC EMC test methods as defined in [2, 5, 7, 9]. They have to fulfill special requirements specified in ETSI and FCC for wireless applications. Therefore these special IC types have to be tested similar to the target application in respect to radiated RF emission and RF immunity.

For ICs targeted for small autarkic wireless applications e.g. remote keyless entry (RKE) or tire pressure monitoring (TPMS) the test effort can be limited to the mandatory radiated tests. Local pin measurements are optional and should be performed only on special request.

B.2 GTEM-cell test board and setup for ICs with RF antenna port

For predicting the IC performance a test board shall be used which carries the IC and all mandatory components but no system components as an antenna. This can be realized with a 50 Ω board which comprises the IC, mandatory elements and a matching network, transforming the impedance of the RF antenna driver/receiver pin to a 50 Ω port. The transformation network has to fulfill the requirements of the IC specification. The 50 Ω port shall be terminated with 50 Ω.

For testing the IC the terminated 50 Ω board is placed in GTEM cell on system level position as shown in Figure 41 and Figure 42, not on IC level position as in [2] and [7]. Therewith, all orientations can be tested. The IC is preferably supplied by a small battery on the test board. The 50 Ω test board as described fully provides emission/sensitivity caused by direct coupling of applied EM fields to the IC or to the mandatory components connected to the IC on the test board without overlaid antenna effects. Therefore this test provides IC level results based on tests similar to application tests without system effects e.g. caused by special antenna characteristics.

During test the IC shall be set in a constant transmitting/receiving mode.

B.2.1 Radiated emission test

For radiated emission 24 test directions should be tested, which means 2 positions top/bottom in 4 directions 0°, 90°, 180°, 270° and in each *x*-, *y*-, z-orientation. The frequencies of interest are the harmonics of the carrier $f_{carrier}$ up to the 10th harmonic of $f_{carrier}$ ($2 \cdot f_{carrier}$, $3 \cdot f_{carrier}$,…, $10 \cdot f_{carrier}$). For each harmonic, the maximum received value is noted of each test direction. Out of all measured radiated field components the equivalent isotropic radiated power (EIRP) value has to be calculated (e.g. with a software tool provided by GTEM cell manufacturer). For one position with the IC in *x*-orientation (see *x*_a in Figure 43) a full scan in the frequency range up to 3 GHz shall be performed for information purpose.

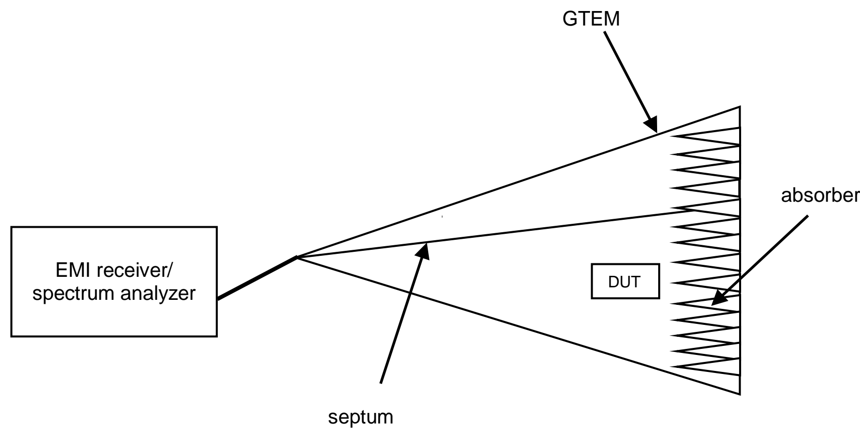

Figure 41: Test setup radiated emission test

B.2.2 Radiated immunity test

For radiated immunity tests, in addition to the IC test board placed on the system level placement in the GTEM cell a receiving antenna has to be placed in GTEM cell nearby the absorbers of GTEM cell. The antenna connecting cable shall be placed along the bottom of GTEM cell and connected via feed trough connectors to the monitoring equipment (e.g. spectrum analyzer). The receiving antenna is used to monitor the carrier of the 50 Ω board during immunity test.

For radiated immunity tests at least 3 to 6 test directions shall be measured (1-2 of each *x*-, *y*-, z-orientation). The test directions shall be selected out of the test directions with the highest level of radiated emission. The test procedure in general can follow IEC62132-2 as the base for radiated immunity tests. As no antenna is applied to 50 Ω board, the carrier is of rather low power but sufficient for monitoring relative behavior of the carrier. Care has to be taken that the monitoring device is not overloaded by the applied field in any frequency range. If the signal from the applied HF source or high harmonics of the HF source is in the monitored frequency band around the carrier of DUT, these test frequencies cannot be tested. These frequencies have to be noted in test report.

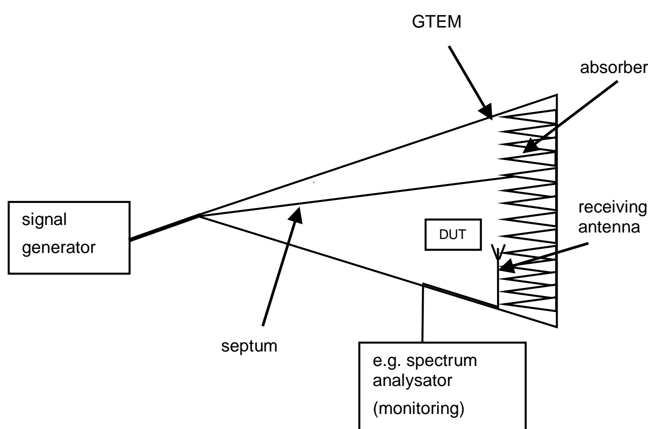

Figure 42: Test Setup Radiated Immunity Test

B.2.3 Positioning and naming of the DUT in GTEM cell

For positioning of the test board with the DUT up to 24 directions are possible, if a rotation angle of 90 degree is used. Some examples and terms are given in the figures below indicating the x-,y-,z- field orientation and DUT position.

If the main positions of the DUT in respect to RF emission or RF reception are known, the test can be limited to these positions.

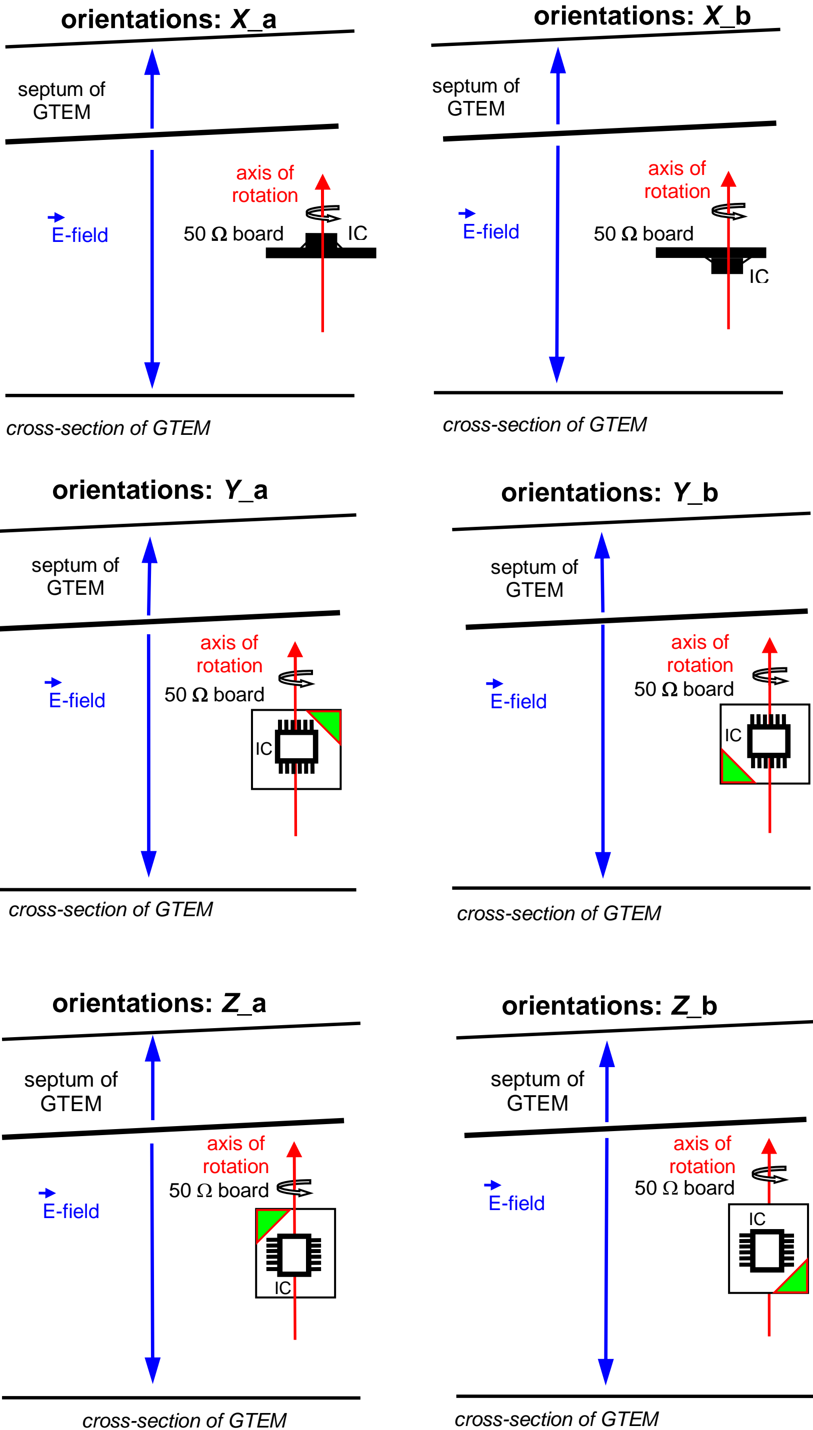

Figure 43: DUT Setup position in GTEM cell

Annex C
Layout recommendation
(informative)

C.1 Several networks

C.1.1 Layout example of 150 Ω networks on 2 layer and multi layer PCB

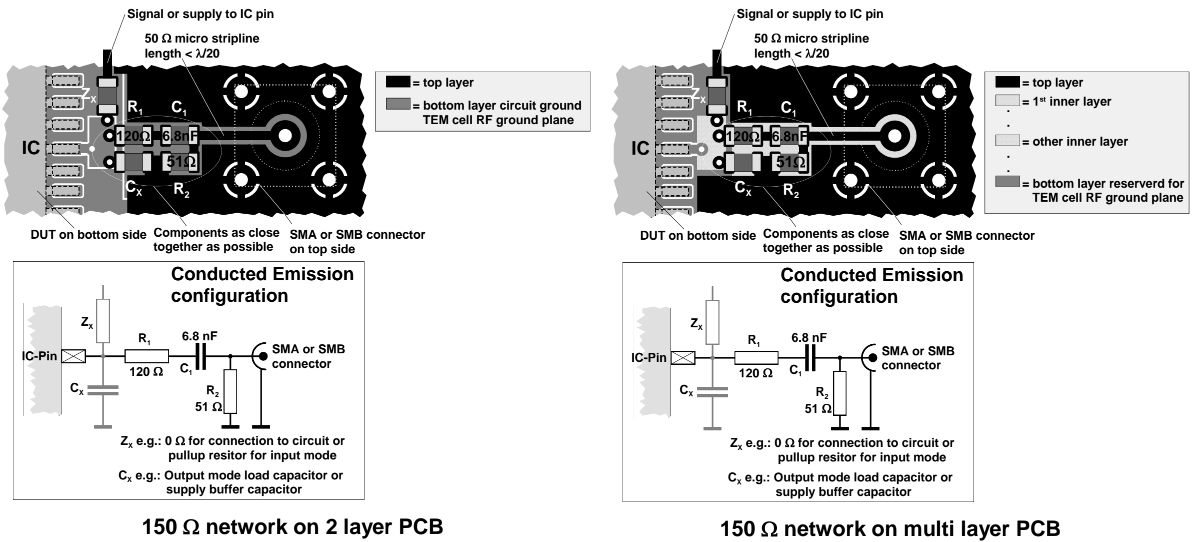

Figure 44: Layout recommendation 150 Ω network

Notes:

- The impedance of the signal island at the IC pin is not 150 Ω, but can be neglected as it is as small as possible.
- This layout recommendation can be configured to perform Direct Power Injection (DPI) according IEC62132-4.
- The distance of the 50 Ω trace edges to the ground copper edges on the same layer should be minimal twice of the distance between the 50 Ω trace and the ground plane underneath the trace.

C.1.2 Layout example of 1 Ω network on 2 layer and multi layer PCB

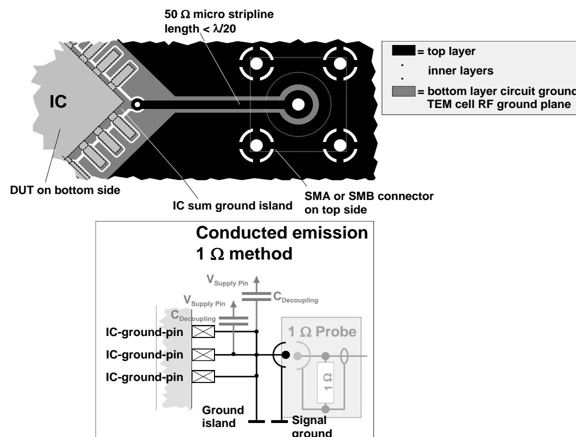

Figure 45: Layout recommendation 1 Ω network

C.1.3 Layout example of DPI network on 2 layer and multi layer PCB

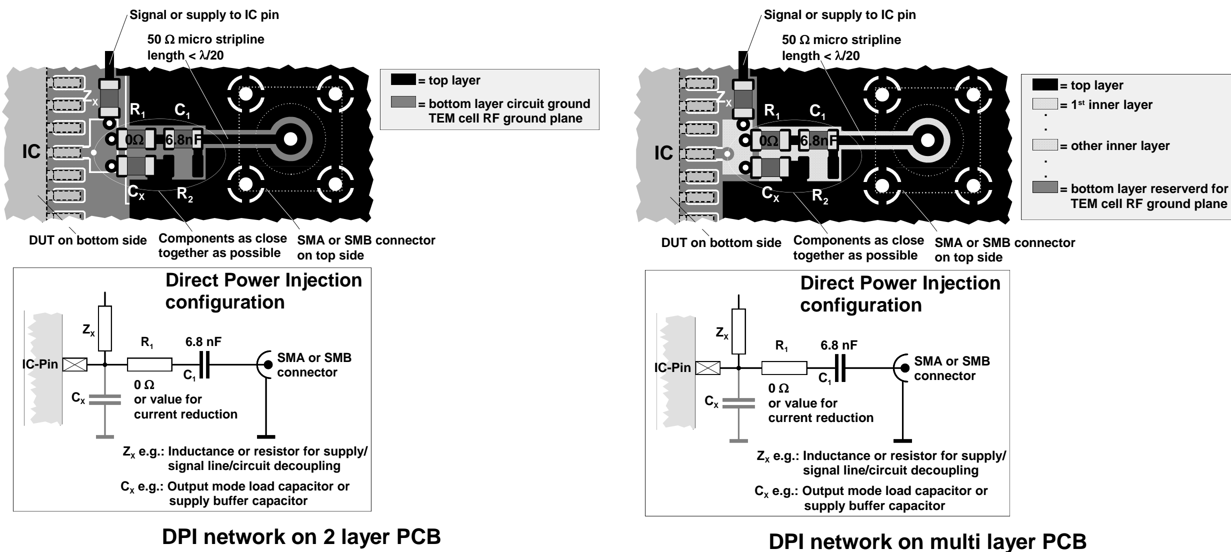

Figure 46: Layout recommendation DPI network

Notes:
- The impedance of signal island at the IC pin is not 50 Ω, but can be neglected as it is as small as possible.
- This layout recommendation can be configured to perform Conducted Emissions according to IEC61967-4.
- The distance of the 50 Ω trace edges to the ground copper edges on the same layer should be minimal twice of the distance between the 50 Ω trace and the ground plane underneath the trace.

C.1.4 Layout Example of a TEM cell test board

The layout requirements for a TEM cell test board are described in detail in [1] and [2].

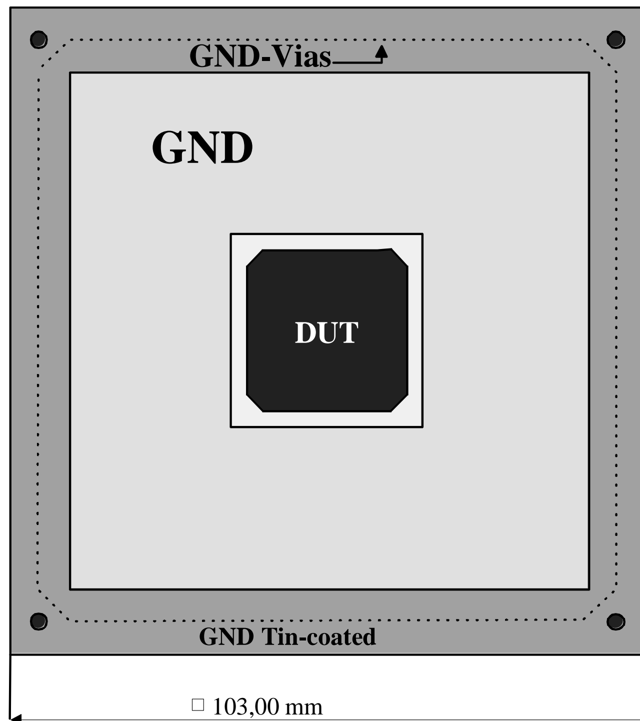

Figure 47: TEM cell test PCB shape

Notes:
- GND-vias are **always** plated through all layers
- all other vias are **partially** plated or buried only

C.1.5 Layout example for systems with IC types *microcontroller, RAM and flash*

In Figure 48 a required 6 layer stack is shown used for systems built with IC types: *microcontroller, RAM* and *flash*:

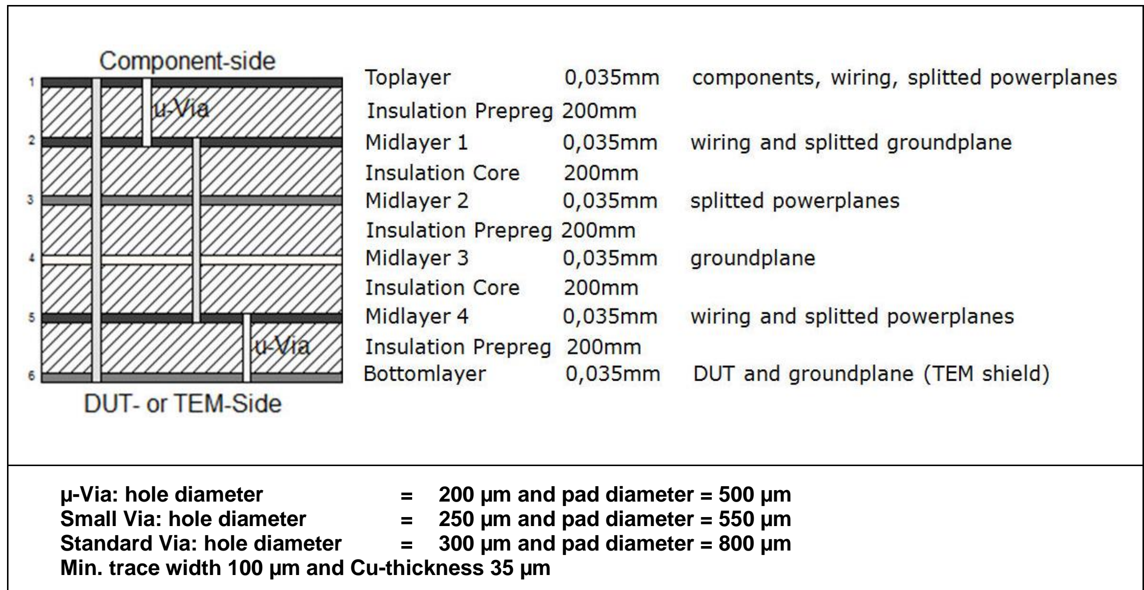

Figure 48: Test board layer stack for systems built of IC types microcontroller, RAM and flash

C.2 Multi method test board

For combined test boards for radiated and conducted tests (conducted emission and DPI) the conducted measurement points and adaptation networks with RF connectors at port pins and supply lines should be realized on the component side of the PCB. Every port pin and every independent power supply that has to be measured needs an adaptation network and a RF connector (e.g. SMA or SMB). Add the conducted test method networks to this board according to the previous chapter.

C.3 Example of multi method test board for microcontrollers

This chapter describes PCB requirements and some layout hints for a combined radiated and conducted methods test board for microcontrollers including external RAM and Flash memory.

C.3.1 Component side (top layer, components, power planes)

To prevent unwanted resonances in the supply system, the wiring recommendation of the different PCB-layers should be followed. Every supply-island is connected with two SMB connectors. One connector is used for measuring the supply voltage according to the 150 Ω method in our example VDDP3 / VEXT for the external-bus/Flash supply-island and VDD for the core supply-island. The other connector which is directly connected with the corresponding supply-island is used for measuring the impedance of the supply-island and the transfer impedance between the supply-islands (in our example X_VDDP3 / X_VEXT for the external-bus/Flash supply-island and X_VDD for the core supply-island). So the split power planes are routed directly on top layer and connected to their corresponding SMB/SMA connectors for spectrum analyzer / network analyzer measurements.

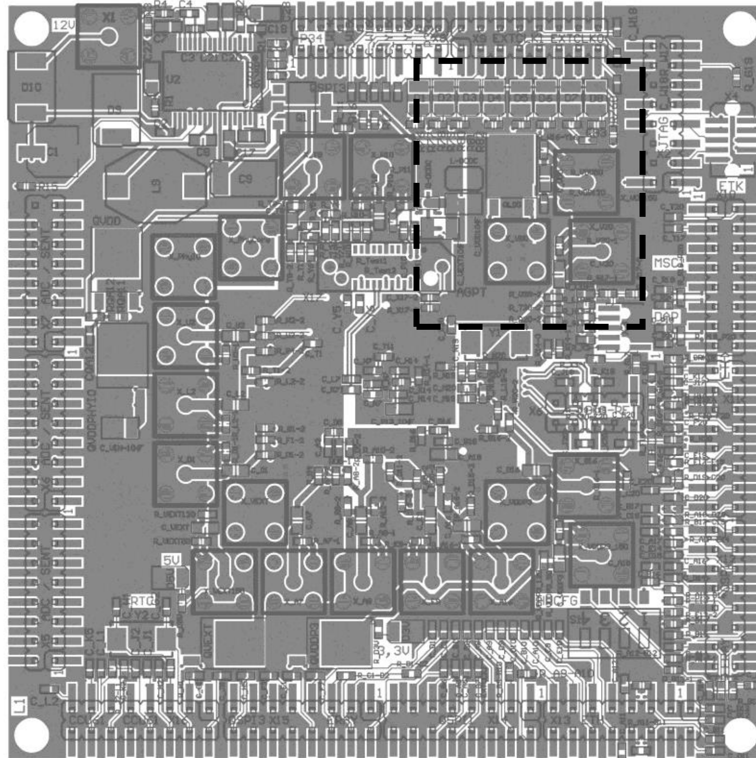

Figure 49: Component side

An integrated voltage regulator has to be placed on the test-board, too. Separated supply-lines to the different islands and component units should be used. Only plated-through holes through all layers and no partial vias shall be used for ground connections. For all other connections only partial vias are allowed. Bus wiring should be limited on component layer and inner layer 4 only. Any wiring between core decoupling capacitors at the component side should be prevented.

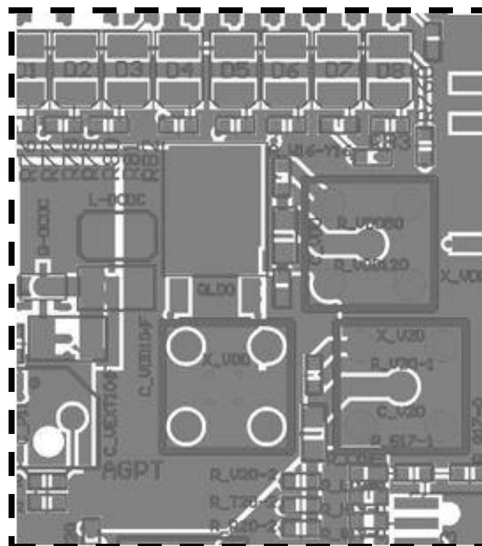

Figure 50: Detail of component side layer

The supply islands are connected by a special land to the supply line at the component side, which makes it possible to separate the island from the supply line very easily. Such an island is shown below in a picture detail of the component side layer.

C.3.2 Inner layer 1 (mid layer 1, ground plane):

The top site signal connections and ground should be at inner layer 1 only. Above inner layer 1 should be wiring of external address, data and bus control signals as well as power planes.

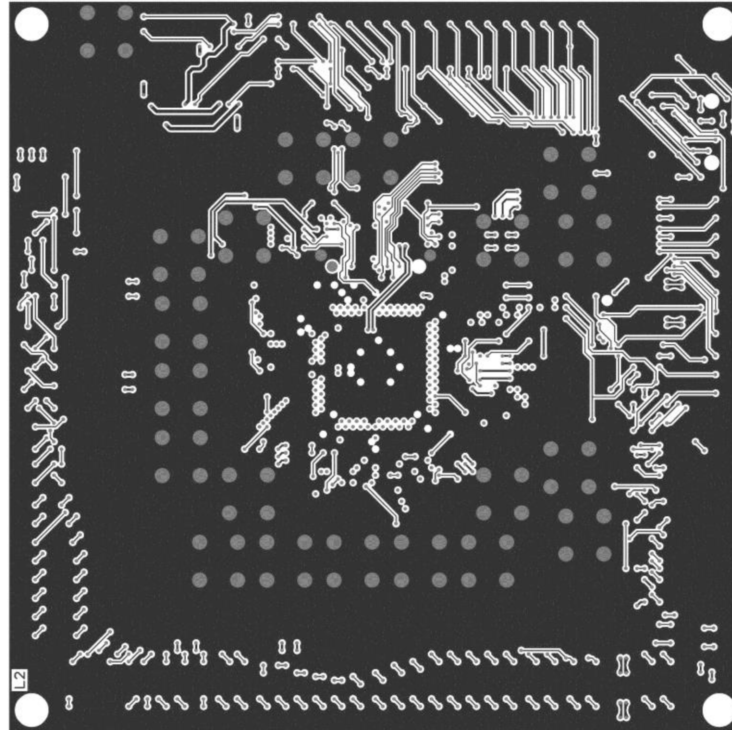

Figure 51: Inner layer 1

C.3.3 Inner layer 2 (mid layer 2, split power planes):

Inner layer 2 should be a split supply plane layer only without any wiring exceptions. Signal and supply vias are basically connected with all layers as far as possible by buried vias.

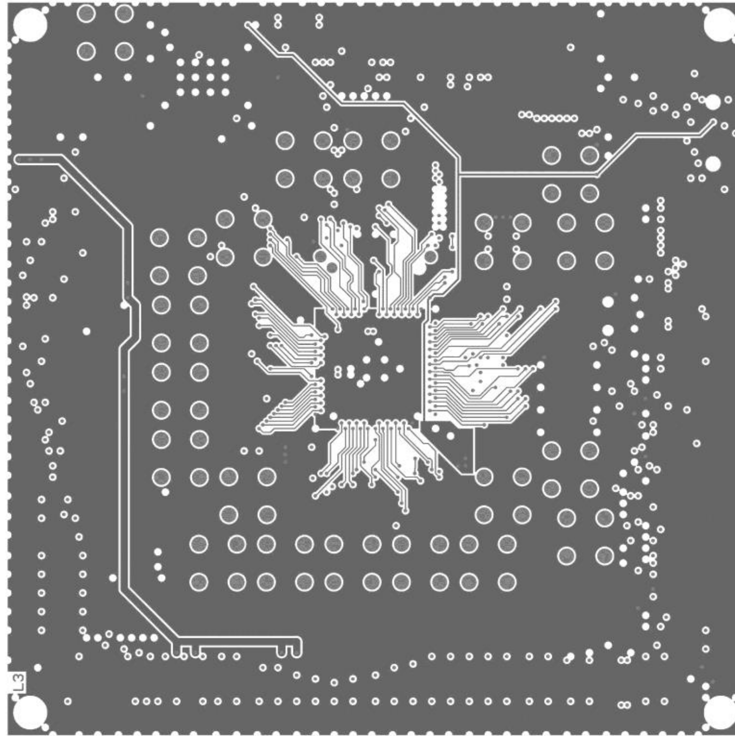

Figure 52: Inner layer 2

C.3.4 Inner layer 3 (mid layer 3, ground plane) :

The main ground island can be placed more favorable at the inner layer 3 with access to buried vias and through hole vias.

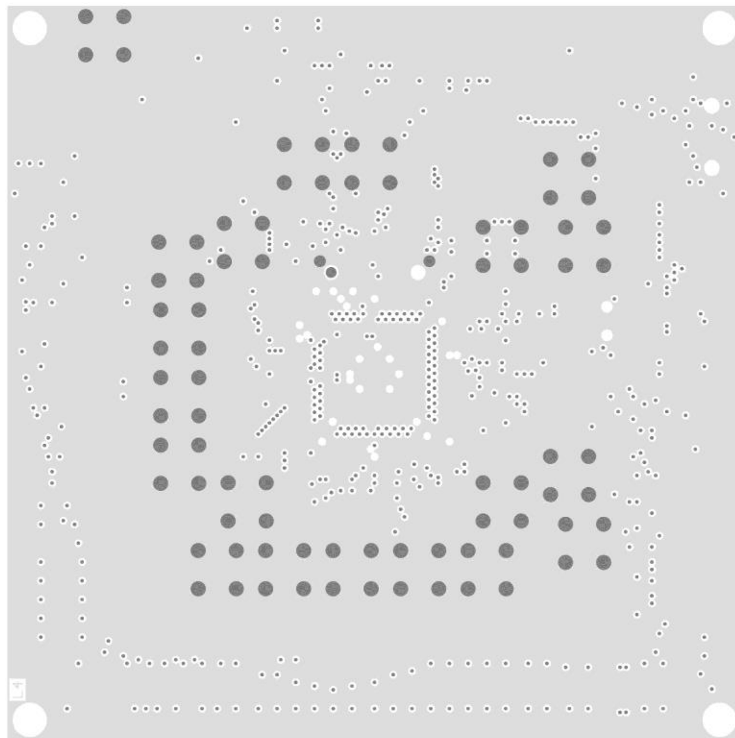

Figure 53: Inner layer 3

C.3.5 Inner layer 4 (mid layer 4, signal wiring, split power plane):

Most of the signal routing should be done in inner layer 4. The wiring of the clock out signal should be between two ground areas in this layer only. USB bus traces for communication purposes are shown in this layer also. An easy access of signal layers is possible from the bottom DUT side by blind vias.

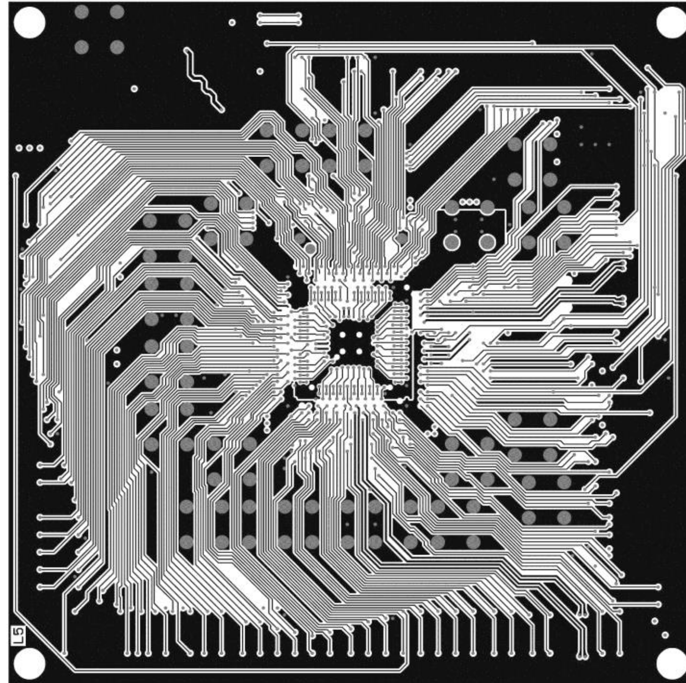

Figure 54: Inner layer 4

C.3.6 Bottom side (DUT, shielding GND for TEM-cell):

Only absolute minimum of wiring should be performed on this layer. Only the DUT (in this example a microcontroller) should be mounted on this layer.

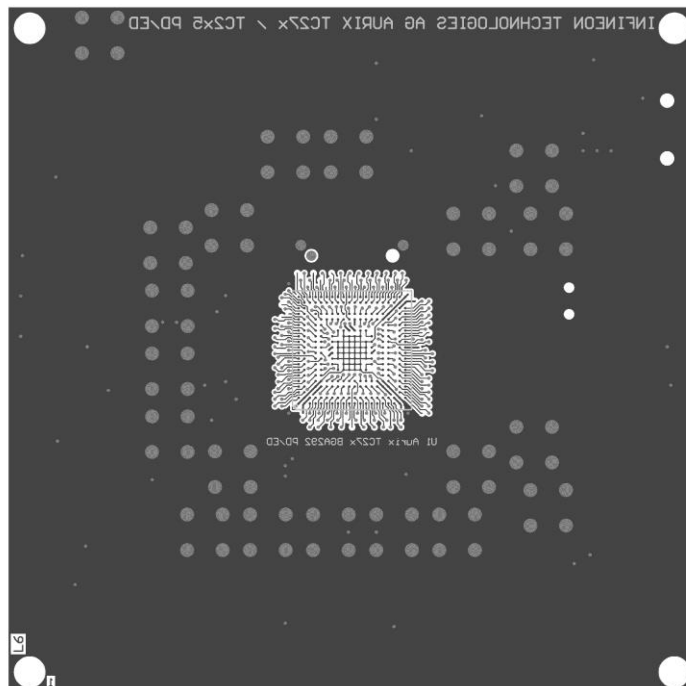

Figure 55: Solder side

C.4 Layout examples of system level ESD test boards

An example of a system level ESD test board with soldered IC used for testing global pins of transceiver ICs is shown in Figure 56.

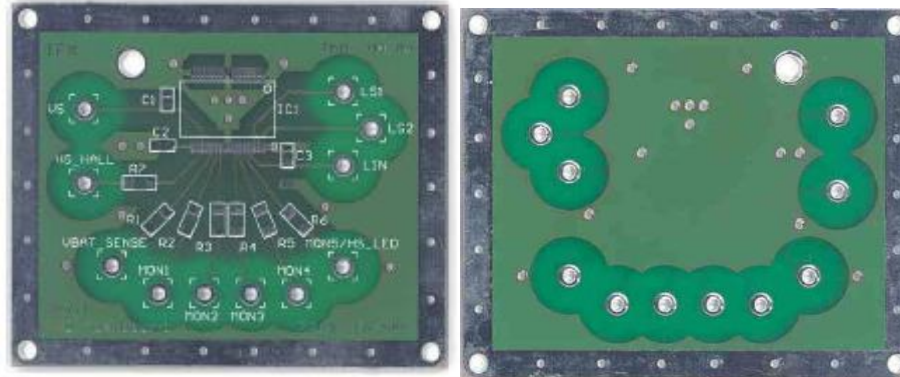

Figure 56: Example of system level ESD test board with soldered IC in top- and bottom layer view

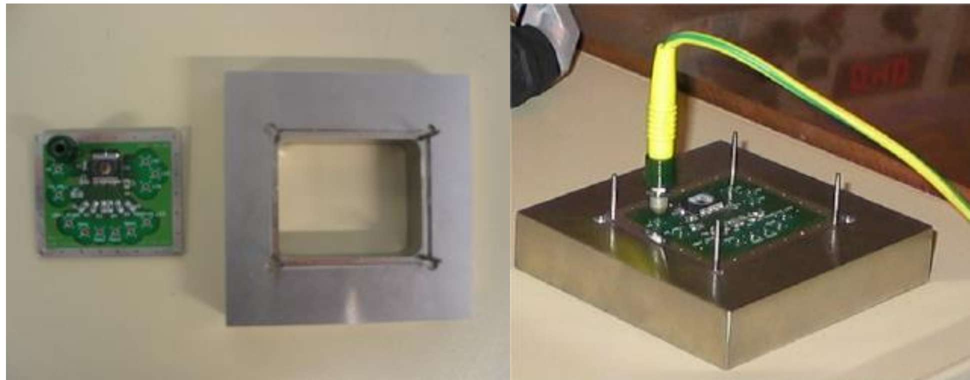

Figure 57: Example of system level ESD test board and fixture

An example of a system level ESD test board with IC connected via socket and external components is shown in Figure 59 to Figure 63.

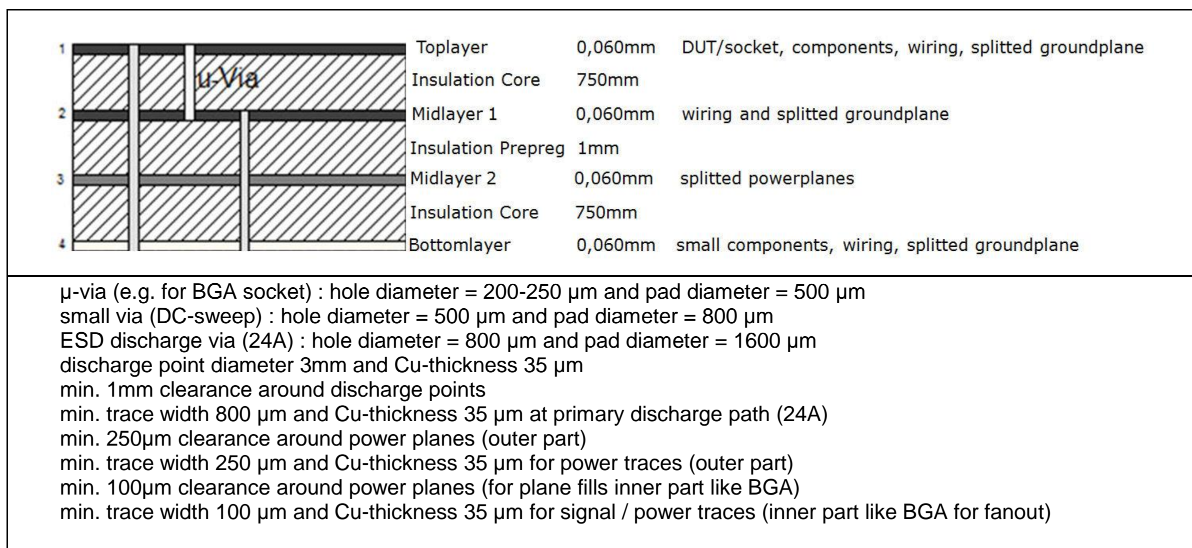

Figure 58: Recommended 4 layer stack up of a test board for IC type microcontroller

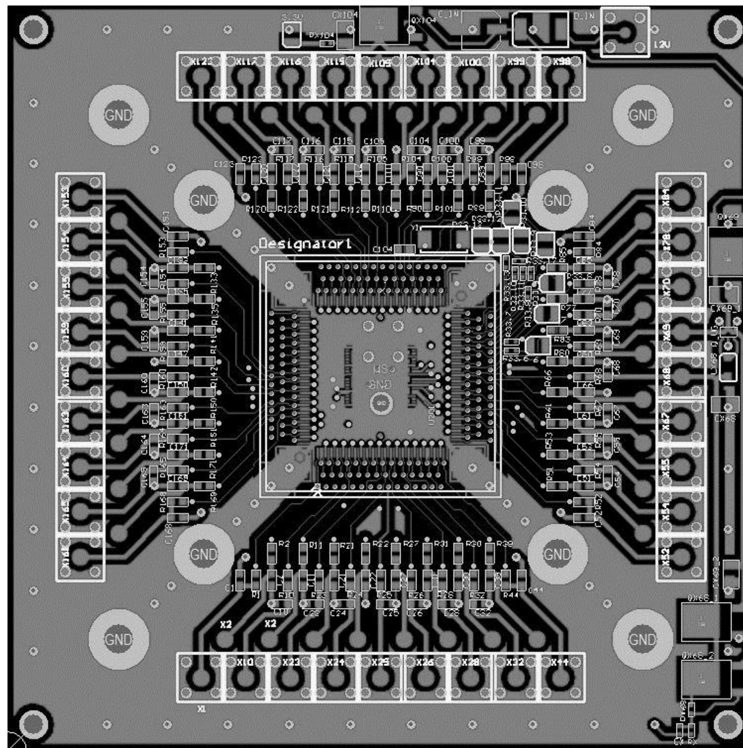

Figure 59: Top layer example of system level ESD test board with microcontroller

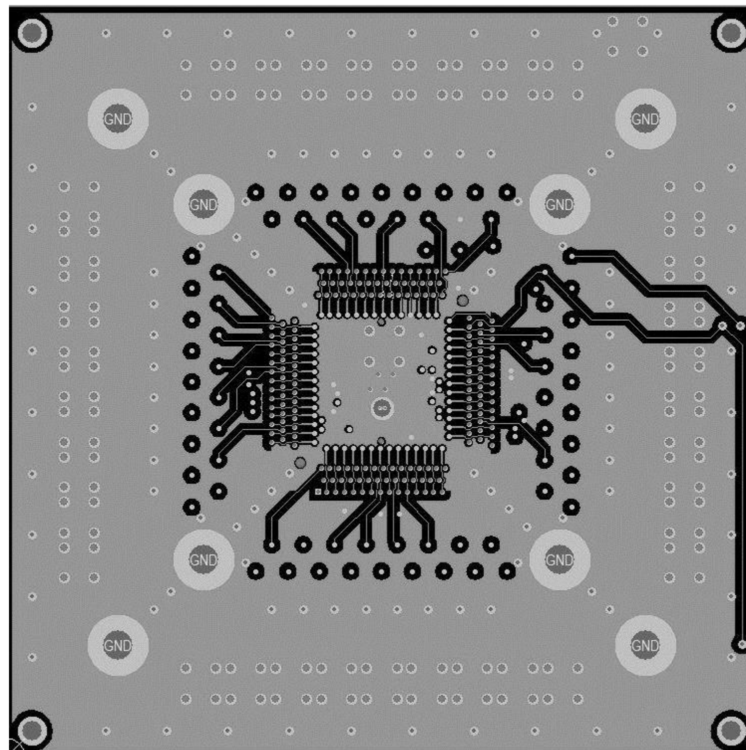

Figure 60: Mid layer 1 example of system level ESD test board with microcontroller

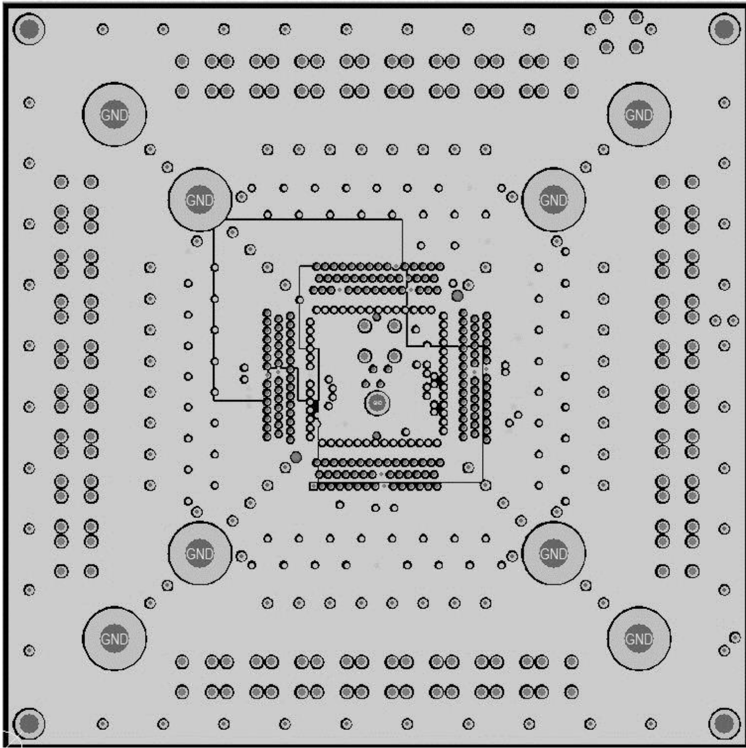

Figure 61: Mid layer 2 example of system level ESD test board with microcontroller

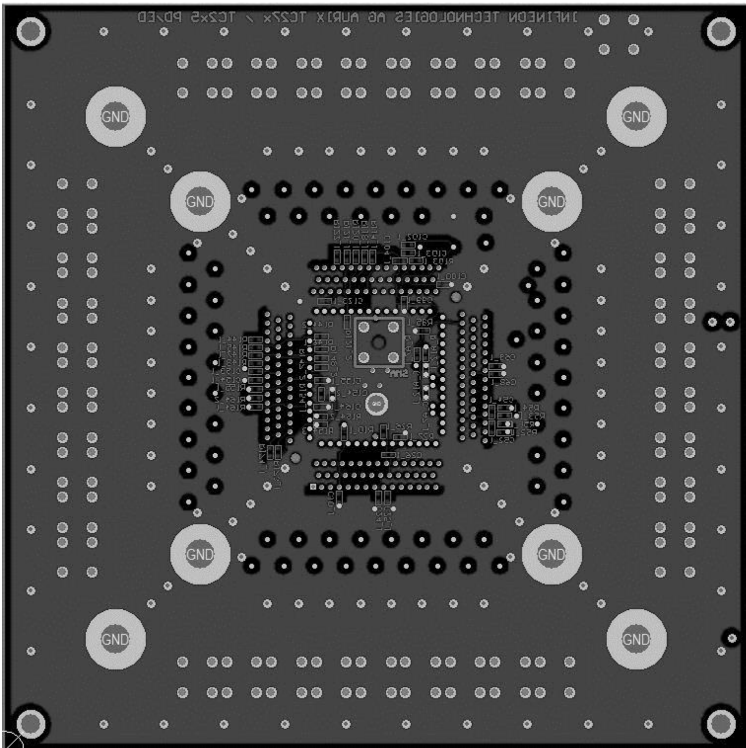

Figure 62: Bottom layer example of system level ESD test board with microcontroller

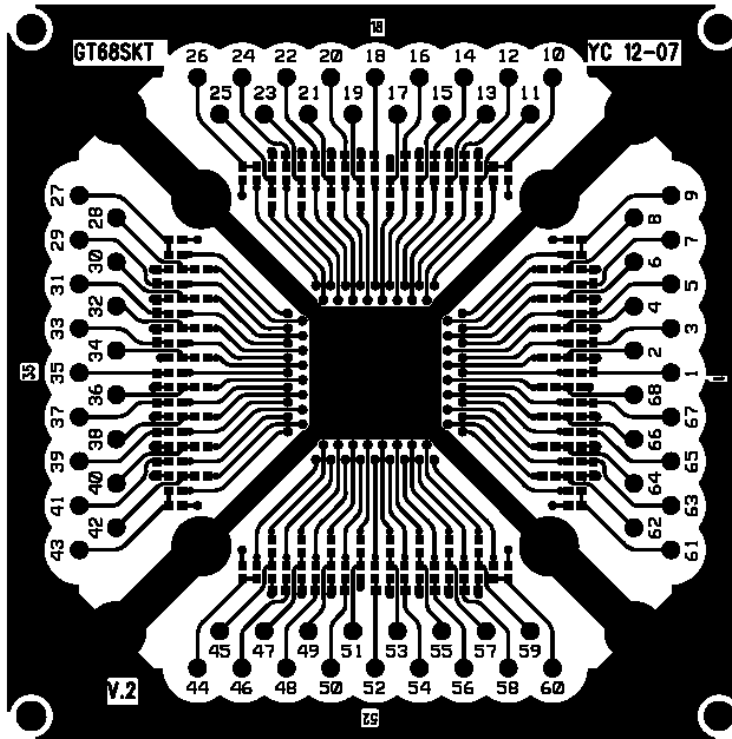

Figure 63: Example of system level ESD test board with IC connected via socket

Annex D
Trace impedance calculation
(informative)

D.1 Equations for calculating micro stripline impedances

These equations should be used for approximation when a field simulator is not available [22]. A field simulator is required for most accurate results.

D.1.1 Micro stripline

$$Z_0 \approx \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \qquad \text{(D1)}$$

valid when $0.1 < \frac{W}{H} < 2.0 \text{ and } 1 < \varepsilon_r < 15$

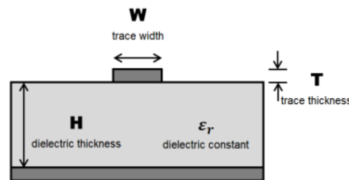

Figure 64: Micro strip line

Note:
- The distance of the 50 Ω trace edges to the ground copper edges on the same layer should be at least twice the distance H between the 50 Ω trace and the ground plane underneath the trace.
- Please consider furthermore that in case of ground copper edges on the same layer the impedance is influenced if varnish is on the PCB surface, too.

D.1.2 Symmetrical stripline

$$Z_{0,sym} \approx \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4H}{0.67\pi(T + 0.8W)}\right) \qquad \text{(D2)}$$

valid when $\frac{W}{H} < 0.35 \text{ and } \frac{T}{H} < 0.25$

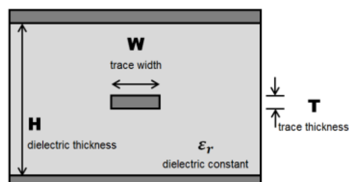

Figure 65: Symmetrical stripline

D.1.3 Offset stripline

The impedance for an offset stripline is calculated from the results of the symmetrical strip line formulas. The reader should note that this formula D3 is an approximation and the accuracy of the results should be treated as such. For more accurate results, use a field solver.

$$Z_{0_{offset}} = 2\frac{Z_{0_{sym}}(2A,W,T,\varepsilon_r)\cdot Z_{0_{sym}}(2B,W,T,\varepsilon_r)}{Z_{0_{sym}}(2A,W,T,\varepsilon_r)+Z_{0_{sym}}(2B,W,T,\varepsilon_r)} \quad \text{(D3)}$$

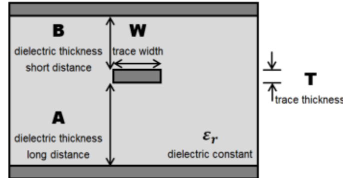

Figure 66: Offset stripline

Note: The distance of the 50 Ω trace edges to the ground copper edges on the same layer should be at least *H*/2 (Figure 65) or B (Figure 66) between the 50 Ω trace and the ground plane underneath/above the trace.

Annex E

Modulation definition for immunity tests (informative)

This annex describes the principle of constant peak test level conservation for modulated signals according to ISO11452-1.

Example for electric field strength:
The electric field strength of the **continuous wave (CW)** signal, E_{CW} may be written in the form

$$E_{CW} = \widehat{E}_{CW} \cdot \cos(\omega t)$$

with $\widehat{E}_{CW}$ peak value of E_{CW}

The mean power may be calculated to

$$P_{CW} = k \cdot \frac{\widehat{E}_{CW}^{\;2}}{2}$$

with k proportionality factor depending on the specific test setup, e.g.

$$k = \frac{h^2}{Z}$$

for the IC stripline with $h =$ height of stripline and $Z = R = 50\Omega$ source impedance.

The electric field strength of an **amplitude modulated (AM)** signal, E_{AM} may be written in the form

$$E_{AM} = \widehat{E}_{CW} \cdot (1 + m \cdot \cos \vartheta t) \cos(\omega t)$$

with ϑ modulation frequency, e.g. $\vartheta = 2 \cdot \pi \cdot 1$ kHz.

Where the peak value is

$$\widehat{E}_{AM} = \widehat{E}_{CW} \cdot (1 + m)$$

The mean power can be calculated by

$$P_{AM} = k \left(1 + \frac{m^2}{2}\right) \cdot \frac{\widehat{E}_{CW}^{\;2}}{2}$$

Note: The total power is the sum of the power in the carrier component and the power in the side- frequency component.

The peak test level preservation may be written as

$$\widehat{E}_{CWpeak} = \widehat{E}_{AMpeak}$$

The relation between CW mean power and AM mean power is then

$$\frac{P_{AM}}{P_{CW}} = \frac{\left[\left(1+\frac{m^2}{2}\right)\cdot\frac{E'^2}{2}\right]}{\frac{E^2}{2}} = \left(1+\frac{m^2}{2}\right)\cdot\left(\frac{E'}{E}\right) = \frac{\left(1+\frac{m^2}{2}\right)}{(1+m)^2}$$

Therefore

$$P_{AM} = P_{CW} \cdot \frac{2+m^2}{2(1+m)^2}$$

For $m = 0{,}8$ (AM 80%) this relation gives $P_{AM} = 0{,}407 \cdot P_{CW}$

In all these formula m is the modulation index, other symbols are explained in the relevant parts of ISO11452.

The electric field strength of an **pulse modulated (PM)** signal, E_{PM} may be written in the form

$$E_{PM} = \begin{cases} \hat{E}_{CW} \cdot \cos(\omega t)\Big|_{0}^{T_{on}} \\ 0\Big|_{T_{on}}^{T} \end{cases}$$

with T_{on} and T according to figure 67.

The r.m.s. value of E_{PM} is

$$E_{PM\,,rms} = \sqrt{\frac{1}{T}\int_0^T E_{PM}{}^2 dt} = \sqrt{\frac{1}{T}\left(\hat{E}^2\int_0^{T_{on}}\cos(\omega t)dt + 0\right)} = \sqrt{\frac{T_{on}}{T}}\cdot\frac{\hat{E}_{CW}}{\sqrt{2}}$$

And the mean power can be written as

$$P_{PM} = k\left(\frac{T_{on}}{T}\right)\cdot\frac{\hat{E}_{CW}}{2}^2$$

For $T_0 = 577\,\mu s$ and $T = 4\,600\,\mu s$ this relation gives $P_{PM} = 0{,}125 \cdot P_{CW}$

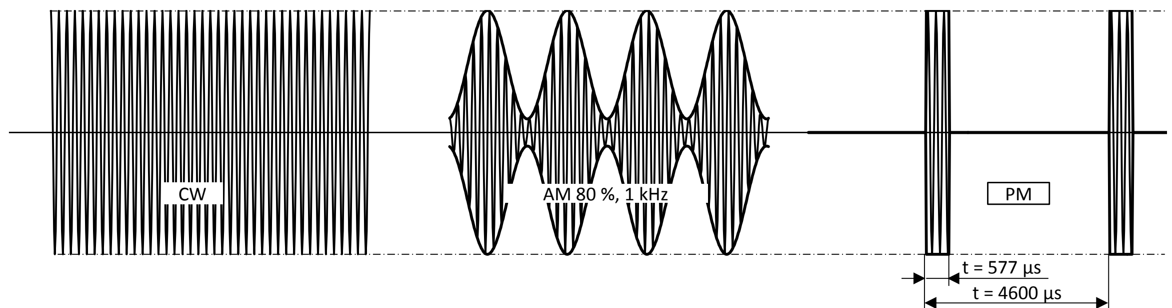

Figure 67: CW signal, AM signal and PM signal for constant peak test level

Annex F
Example of an IC EMC specification (informative)

IC type with CPU, emission

coupling point							coupling mechanism				test method selection with limit (class I-III,C,C-BS)		
pin (if available)			IC function module	pin type (global/local)	functional configuration	operation mode*	direct	port crosstalk	core crosstalk	osc. crosstalk	150 Ω	1 Ω	(G)TEM IC-stripline
no.:	name	function											
all signals for external (synchronous and asynchronous) memory access													
		system clock output	regional driver	local	C1	S2							III
		data bus	regional driver	local	C1	S2							III
		address bus	regional driver	local	C1	S2							III
		ALE signal pin	regional driver	local	C1	S2							III
		all chip select (CS)	regional driver	local	C1	S2							III
		read (R)	regional driver	local	C1	S2							III
		write (W)	regional driver	local	C1	S2							III
		other memory access signals	regional driver	local	C1	S2							III
digital ground													
		GNDD1..x	supply	global	C1	S2						III	III
supplies													
		Vcc_core1..x	supply	global	C1	S2			•		III		III
		Vcc_osc	supply	global	C6	S1				•	III		III
		Vcc_I/O	supply	global	C1	S3		•			III		III
synchronous serial bus (e.g.SPI, I^2C)													
		communication clock out (e.g. SPI CLK)	regional driver	local	C1	S3	•				III		III
		com. data out (e.g. MOSI)	regional driver	local	C1	S3	•				III		III
I/O port with highest driver strength													
		digital I/O port in output mode	regional drivers	local	C5-S3	T							III
					C5-S3	H,L, IA		•	•	•	III		III
					C1-S2	H,L, IA			•	•	III		III
input port													
		digital (I/O) port in input mode	regional receivers	local	C5-S3	H,L, IA		•	•	•	III		III
			regional receivers	local	C1-S2	H,L, IA			•	•	III		III
		analog port in input mode	regional receivers	local	C5-S3	H,L, IA		•	•	•	III		III
			regional receivers	local	C1-S2	H,L, IA			•	•	III		III
line drivers and line receivers													
		relay drivers	line drivers	global	C5-S3	T	•				III		III
					C5-S3	H,L		•			III		III
					C1-S2	H,L			•	•	III		III
		'Wake up' signal	line receivers	global	C1-S2	IA			•	•	III		III

coupling point							coupling mechanism				test method selection with limit (class I-III,C,C-BS)		
pin (if available)			IC function module	pin type (global/local)	functional configuration	operation mode*	direct	port crosstalk	core crosstalk	osc. crosstalk	150 Ω	1 Ω	(G)TEM IC-stripline
no.:	name	function											
asynchronous serial bus (e.g. CAN)													
		CAN driver	symmetrical line drivers	global	C5-S3	T	•				III		III
					C5-S3	H,L		•			III		
					C1-S2	H,L			•	•	III		
		CAN receiver	symmetrical line receivers	global	C1-S2	IA			•	•	III		III

Table 50: IC EMC specification, IC type with CPU, emission

***) Note:** T = toggle; H = static high potential, L = static low potential, A = defined active; IA = defined inactive (e.g. open drain mode passive, tristate), realised with internal or external pull up or pull down

IC type with CPU, immunity

injection point							monitoring				test method					
pin				pin type (global/local)	configuration mode*)	operation mode*)	monitoring pins			failure criteria	DPI			(G)TEM IC-stripline		
no.	name	function	port IC function module				no.	name	function		CW	AM	PM	CW	AM	PM
		reset	regional input	local	C10	S3			I/O port	1	II	II	II			
					C10	S3			reset	2	II	II	II			
PLL configuration pins																
		PLL-freq1..x	regional input	local	C10	S3			CLK out or toggling port	1	II	II	II			
											II	II	II			
											II	II	II			
I/O output pins																
		IA open drain	regional output	local	C10	S3			I/O port	3	II	II	II			
		H,L	regional output	local	C10	S3			I/O port	3	II	II	II			
		T	regional output	local	C10	S3			I/O port	3	II	II	II			
oscillator																
		Xtal1	oscillator	local	C11	S3			CLK out or toggling port	1	I	I	I			
		Xtal2		local							I	I	I			
supplies																
		Vcc_core1..x	supply	global	C10	S3			I/O port	1	III	III	III			
		Vcc_osc	supply	global	C10	S3			CLK out or toggling port	1	III	III	III			
		Vcc_I/O	supply	global	C10	S3			I/O port	1	III	III	III			
entire IC																
					C10	S3			I/O port	1				III	III	III

Table 51: IC EMC specification, IC type with CPU, part 1 immunity

***) Note:** T = toggle; H = static high potential, L = static low potential
A = defined active; IA = defined inactive, realised with internal or external pull up or pull down

Failure criteria

failure criterion no.	monitored function	failure criteria
1	toggling port	frequency ±3%
2	voltage at pin	as specified in data sheet ±10%

Table 52: IC EMC specification, IC type with CPU, part 2 failure criteria

Pulse immunity

injection point							monitoring				test method
pin				pin type (global/local)	functional configuration	operation mode*)	monitoring pins			failure criteria	transients on supply
no.	name	function	port IC function module				no.	name	function		
example:											
		reset	regional input	local	C1-S2	A			I/O Port	1	III
					C1-S2	A			reset	2	III
		PLL-freq1..x	regional input	local	C1-S2	A			CLK out or toggling port	1	III
											III
											III

Table 53: Structure of an IC EMC specification, part 1 pulse immunity

***) Note:** T = toggle; H = static high potential, L = static low potential
A = defined active; IA = defined inactive, realized with internal or external pull up or pull down

Failure criteria

failure criterion no.	monitored function	failure criteria
1	toggling port	frequency ±3%
2	voltage at pin	as specified in data sheet ±10%

Table 54: Structure of an IC EMC specification, part 2 pulse immunity

System level ESD

pin no.	name	function	external components	ESD Level
example:				
3	OUT	low side driver	none	I
7	VCC	supply	100 nF to GND	II
12	LIN	line driver	diode	III

Table 55: Structure of an IC EMC specification, part system level ESD

Annex G
Calculation of pin specific limits
(informative)

G.1 Fourier transformation of time domain signals

Toggling digital data pins or periodically switching analog power outputs generate switching harmonics as a matter of principle defined by the functionally necessary and specified signal waveform. The resulting harmonics of those wanted signal waveforms can be calculated with Fourier-transformation.

For trapezoidal periodic signals as shown in Figure 68, the envelope of the resulting amplitude versus frequency spectrum can be subdivided into 3 sections. From the fundamental frequency of the signal up to the first corner frequency f_{g1} the spectral response is parallel with the frequency axis. After the first corner frequency f_{g1} the amplitudes diminish up to the second corner frequency f_{g2} with 20 dB/decade. From this point the spectrum decreases with 40 dB/decade, as shown in Figure 68. The simplified equations to calculate amplitudes and corner frequencies of the spectrum are shown in Figure 69. A_O is defined as the amplitude of original signal (I or V), t_i as the signal pulse width, t_s as the switching time, T_O as the period of the fundamental frequency and n as the multiples of the fundamental frequency.

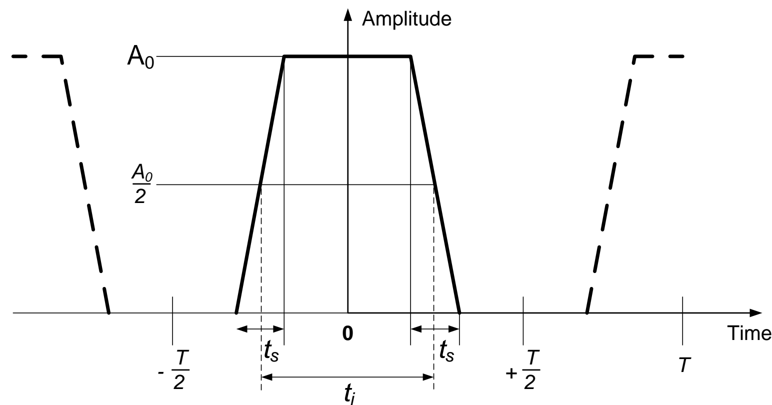

Figure 68: Periodical trapezoidal signal, time domain

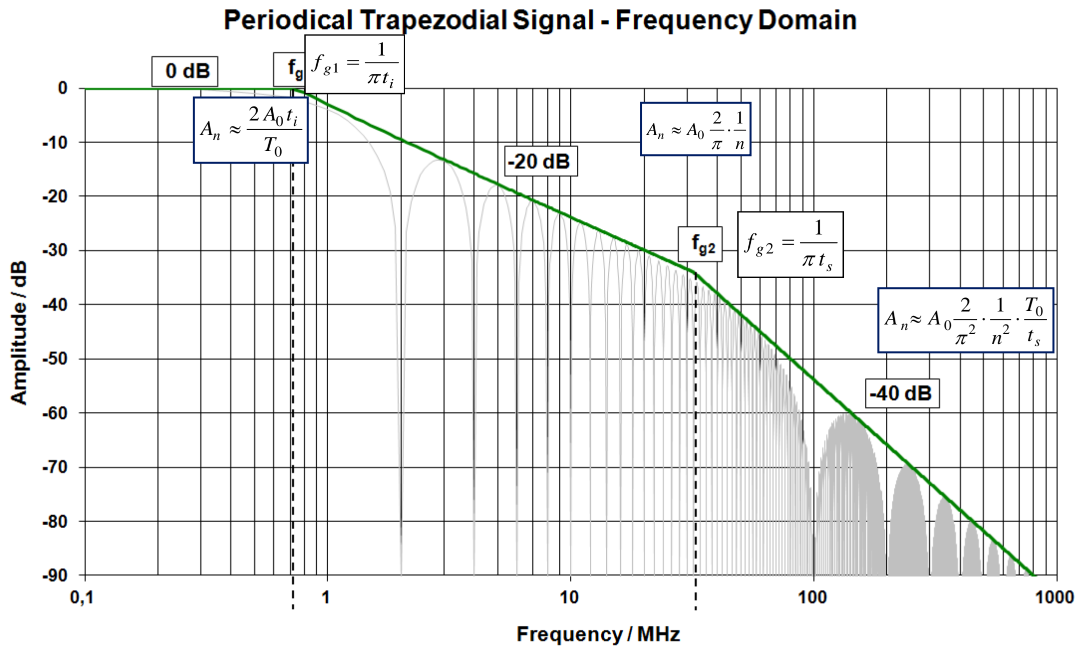

Figure 69: Fourier analysis of periodical signals (simplified calculation)

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