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DeQuMa - Tutorial

How to use the ZVEI - DeltaQualificationMatrix

Stand 21.07.2022 | DeQuMa Revision 5

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

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What is the DeQuMa?

It‘s a tool to describe the requested change, the evaluation level and the test which should be considered for qualification based on common international standards (AEC-Q10x, AEC-Q200).

Motivation – Why to use?

Standardized scope of Qualification for selection of tests.
Common understanding for tests and changes will decrease the PCN throughput time.

Do not use for Information Notes!

The DeQuMa should only be submitted in case of changes which are assessed as “P”.
For changes which are assessed as “I” the DeQuMa is not necessary.

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

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Content of the DeQuMa (Overview file folders / sheets)

14		SEM-DS-02	Correction of data sheet or issue of errata	I	I	Please indicate clearly, that Infonote co type of change! Assessment in application required!
		SEM-DS-03	Specification of additional parameters	I	P	Description of a new not previously cov parameter. No technical change of the **(I):** Definition of new parameter which w

Guidance | History | **Active Components** | Optoelectronic Components | MEMS | MCM | Passive Components

Bereit

further instructions and descriptions

DeQuMa Releases

matrix for Active Components (AEC-Q100 and AEC-Q101)

matrix for Optoelectronics (AEC-Q102)

matrix for MEMS (AEC-Q103)

matrix for MCM (AEC-Q104)

matrix for Passive Components (AEC-Q200)

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

Example - DeQuMa for Active Components

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Worked on: (Name, Function) Max Mustermann
Signature:
Date:
PCN number:
For integrated circuits or discrete semiconductors select below: AEC-Q100 Revision H

1b

Hide Text
Values: Hide Rows
Values: Hide Columns

Guidance | History | Active Components | Optoelectronic Components | MEMS | MCM | Passive Components

1a

Bereit

1a) Select respective file folder

1b) Select in Active Component folder if AEC Q100 or 101 is applicable and complete Header Data

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

Example - DeQuMa for Passive Components

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Worked on: (Name, Function): Max Mustermann
Signature:
Date:
PCN number:

Hide Text
Values: Hide Rows
Values: Hide Columns

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Mark change with an "x"

1c

Selection of component

ID	Type of change	Potential impact?	Understanding of component experts	Examples to explain	Evaluation level A / B / C	Further applicable conditions	Line evaluation (can be evaluated by data or audit/on site check)	AEC-Q200 Revision D	Check of specification (for raw material only)	High Temp Exposure (Storage)	Temperature Cycling
	NETWORKS & RESISTORS										
	ANY										
PAS-RES-AN-01	Any change with impact on agreed upon	P	Intended to be used if no other type of change is applicable but the change affects agreed technical contractual agreements.	Not relevant for technical evaluation.	*		-	-	-	-	-
PAS-RES-AN-02	Any ch... ...th impact on processability the matrix ...	P		Technical interface means component terminals.	B		-	-	-	-	-
	DATA SHEET										
PAS-RES-DS-01	Change of data sheet paramete... specification	P	Change of application relevant information **Not included:** Editorial changes.	e.g. tighten of electrical parameter distribution	A	Risk assessment depending on change for each application.	-	-	-	-	-
PAS-RES-DS-02	Correction of data sheet or issue of errat...	I	No technical change of product, process or test. New description of behavior which was not specified before or which is different from initial specification. Please indicate clearly, that Infonote contains this type of change! Assessment in application required!!	e.g. data sheet correction because of new information about component behavior	A		-	-	-	-	-
PAS-RES-DS-03	Specification of additional parameters	P	Description of a new not previously covered parameter. No technical change of the product. **(I):** no influence **(P):** Risk assessment depending on change for each application to provide evidence of additional parameters (stat. evaluation)	e.g. adding new (tested) parameter.	A		-	-	-	-	-

Assessment of impact regarding following aspects
- contractual agreements
- technical interface of handling/processability/manufacturability of customer
- form, fit, function, quality performance, reliability

Evaluation level: A: Application level; B: Boardlevel; C: Component level; *: Not relevant for qualification matrix

Von A bis Z sortieren
Von Z bis A sortieren
Nach Farbe sortieren
Tabellenansicht
Filter löschen aus "Selection of com..."
Nach Farbe filtern
Textfilter
Suchen
(Alles auswählen)
Al-Cap
CERAMIC / TANTALUM
Film capacitors
INDUCTORS
NETWORKS & RESISTORS
NTC
PTC
QUARTZ CRYSTAL / SAW
VDR
OK
Abbrechen

For **Passive** components:

1c) in Order to reduce the number of lines (> 400) select a product group first

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

Example - DeQuMa for Active Components

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Worked on: (Name, Function)	Max Mustermann
Signature:	
Date:	
PCN number:	
For integrated circuits or discrete semiconductors select below:	AEC-Q100 Revision H

Hide Text

Values: Hide Rows | Values: Hide Columns

Form provided by ZVEI - Revision 5.0 - December 2021

Mark change with an "x"

Assessment of impact regarding following aspects
- contractual agreements
- technical interface of handling/processability/manufacturability of customer
- form, fit, function, quality performance, reliability

MATERIAL PERFORMANCE: Includes integrated circuits (e.g. ASICs, µ-Controller…

Mark	ID	Type of change	Potential impact? No	Potential impact? Yes	Understanding of semiconductors experts	Examples to explain	Evaluation level A / B / C	Further applicable conditions	Line evaluation (can be evaluated by data or audition site check)	AEC-Q100 Revision H	Check of specification (for raw material only)	A2 THB	A3 AC	A4 TC	A5 PTC	A6 HTSL	B1 HTOL	B2 ELFR	B3 EDR	C1 WBS	C2 WBP
		ANY																			
	SEM-AN-01	Any change with impact on agreed upon technical contractual agreements	P	P	Intended to be used if no other type of change is applicable but the change affects agreed technical contractual agreements.		*		-	-	-	-	-	-	-	-	-	-	-	-	-
	SEM-AN-02	Any change with impact on processability/manufacturability at customer, which is not covered in the matrix below.	P	P	Any change which is not covered in the matrix below, but risk assessment at customer is recommended.		B		-	-	-	-	-	-	-	-	-	-	-	-	-
		DATA SHEET																			
	SEM-DS-01	Change of data sheet parameters/electrical specification (min./max./typ. values) and/or AC/DC specification	P	P	Update of data sheet because of technical change of the product.	e.g. recommendations for pull-up/pull-down or NC pins, MSL	A		-	-	-	-	-	-	-	-	-	-	-	-	-
	SEM-DS-02	Correction of data sheet or issue of errata	I	I	No technical change of product, process or test. New description of behavior which was not specified before or which is different from initial specification. Please indicate clearly, that Infonote contains this type of change! Assessment in application required!	e.g. Errata	A		-	-	-	-	-	-	-	-	-	-	-	-	-
	SEM-DS-03	Specification of additional parameters	I	P	Description of a new not previously covered parameter. No technical change of the product. **(I):** Definition of new parameter which was not documented before. **(P):** Not known as single change. Only in combination with other changes.	(I): e.g. adding new tested parameter.	A		-	-	-	-	-	-	-	-	-	-	-	-	-
		DESIGN																			
x	SEM-DE-01	Design changes in active elements. [1])	P	P	Any device relevant changes in design / layout of elements with effect on specified electrical behavior. [1]) **Not included:** Modification to adjust product parameter within specified process window and design rules.	e.g. change of ESD structure, add / remove a transistor in layout	A	Please check if data sheet is affected **(SEM-DS-01)**.	-	•	-	-	•	•	M	-	•	•	D,J	-	-
	SEM-DE-02	Design changes in routing. [2])	P	P	Any change of wiring between elements in chip design / layout with effect on specified electrical behavior. [2]) **Not included:** Modification to adjust product parameter within specified design rules.	e.g. mask changes in metal fix for corrective action (based on external 8D report) e.g. Connecting / disconnecting an already existing transistor through routing	C	**A:** Impact on EMC behavior cannot be evaluated / excluded on component level. **A:** If impact on electrical function is not excluded on component level. Please check if data sheet is affected **(SEM-DS-01)**.	-	•	-	-	-	A	M	-	-	-	-	-	-
	SEM-DE-03	Die shrink [3])	P	P	Shrink of active area. [3]) **Not included:** sawing street/kerf/scribe line	Typical shrink of die.	A	Please check if change in process technology **(SEM-PW-09)** is also affected.	-	•	-	•	•	-	M	-	•	•	D,J	-	-
					Integrated software by design or memory as…																

Evaluation level: A: Application level, B: Boardlevel, C: Component level, *: Not relevant for qualification matrix

2 | 3

2) Select all changes for the PCN in column B.

ATTENTION !

ALL changes per PCN need to be marked in column B by ‚X'….

3) If the wording for the change category you selected (column D) is not clear enough, you will find additional explanations for the specific category in column G and H.

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

Example - DeQuMa for Active Components

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Worked on: (Name, Function): Max Mustermann

Signature:

Date:

PCN number:

For integrated circuits or discrete semiconductors select below: AEC-Q100 Revision H

Show Text

Values: Show Rows

Values: Show Columns

i.

ii.

iii.

Assessment of impact regarding following aspects
- contractual agreements
- technical interface of handling/processability/manufacturability of customer
- form, fit, function, quality performance, reliability

Mark change with an "x"

Device evaluation

MATERIAL PERFORMANCE TEST RESULTS (on the basis of AEC-Q100 Revision H)

Includes integrated circuits (e.g. ASICs, µ-Controller, memories, voltage regulators, smart power devices, logic devices, analog devices, ...)

	ID	Type of change	Potential impact? No	Potential impact? Yes	Evaluation level A / B / C (A: Application level, B: Boardlevel, C: Component level, *: Not relevant for qualification matrix)	AEC-Q100 Revision H	Check of specification (for raw material only)	Temperature Humidity Bias or biased HAST THB A2	Autoclave or Unbiased HAST AC A3	Temperature Cycling TC A4	Power Temperature Cycling PTC A5	High Temperature Storage Life HTSL A6	High Temperature Operating Life HTOL B1	Early Life Failure Rate ELFR B2	NVM Endurance, Data Retention, and Operational Life EDR B3	Wire Bond Shear WBS C1	Wire Bond Pull WBP C2	Solderability SD C3	Lead Integrity LI C6	Electromigration EM D1	Time Depending Dielectric Breakdown TDDB D2	Hot Carrier Injection HCI D3	Negative Bias Temperature Instability NBTI D4	Stress Migration SM D5	Electronic Discharge Human Body Model HBM E2	Electronic Discharge Charged Device Model CDM E3	Latch up LU E4	Electrical Distribution ED E5	Characterisation CHAR E7	Electromagnetic Compatibility EMC E9	Short Circuit Characterization SC E10	Soft Error Rate SER E11	Lead free LF E12	Hermetic Package Test MECH G1-4	Package Drop DROP G5	Die Shear DS G7
		ANY																																		
		DATA SHEET																																		
		DESIGN																																		
x	SEM-DE-01	Design changes in active elements. [1])	P	P	A	•	-	-	•	•	M	-	•	•	D,J	-	-	-	-	D	D	D	D	D	•	•	•	•	•	•	•	•	-	-	F	-
		PROCESS - WAFER PRODUCTION																																		
x	SEM-PW-03	New final wafer thickness	P	P	C	•	-	-	-	E	M	-	•	•	-	E	E	-	-	-	-	-	•	-	E	E	E	•	-	-	-	-	-	-	-	-
		BARE DIE (Wafer process changes not covered in this section shall be handled according to section "PROCESS - WAFER PRODUCTION")																																		
		PROCESS - ASSEMBLY																																		
x	SEM-PA-05	Change of lead and heat slug plating material/plating thickness (external)	P	P	B	•	•	•	•	•	M	•	-	-	-	-	C	•	•	-	-	-	-	-	-	-	-	-	-	-	-	-	L	H	-	H
		PACKING/SHIPPING																																		
		EQUIPMENT																																		
		TEST FLOW																																		
		Q-GATE																																		
		Tests, which should be considered for the appropriate process change.			A	•	•	•	•	E,•	M	•	•	•	D,J	E	C,E	•	•	D	D	D	D,•	D	E,•	E,•	E,•	•	•	•	•	•	L	H	F	H

Improved readability by toggle buttons (Hide/Show):

i. **Hide Text compresses columns G, H and J**

ii. **Values: Hide Rows filters the change lines only**

iii. **Values: Hide Columns compresses MATERIAL PERFORMANCE TEST RESULTS columns for ‚-‘ listed stress tests**

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

Example - DeQuMa for Active Components

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Understanding of semiconductors experts	Examples to explain	Evaluation level A / B / C (A: Application level, B: Boardlevel, C: Component level, *: Not relevant for qualification matrix)	Further applicable conditions	AEC-Q100 Revision H	Check of specification (for raw material only)	Temperature Humidity Bias or biased HAST THB A2	Autoclave or Unbiased HAST AC A3	Temperature Cycling TC A4	Power Temperature Cycling PTC A5	High Temperature Storage Life HTSL A6
Any device relevant changes in design / layout of elements with effect on specified electrical behavior. *) Not included: Modification to adjust product parameter within specified process window and design rules.	e.g. change of ESD structure e.g. add / remove a transistor in layout	A	Please check if data sheet is affected **(SEM-DS-01)**.	•	-	-	•	•	M	-
Change in final wafer thickness.	e.g. change in final chip/die thickness	C	**A:** If ther[…] is affected (like MOSFET; IGBT, BGA package[…] **A:** If imp[…] behavior cannot be evaluated / excluded […]	•	-	-	-	E	M	-
SS - WAFER PRODUCTION")										
Change in material and / or process resulting in a new technology (e.g. pure tin).	e.g. change in heat slug stack e.g. change from Sn into Ni/Pd/Au e.g. change of layer thickness e.g. change of external bumps of a BGA e.g. Change of external pins of a hermetic package	B		•	•	•	•	•	M	•
		A		•	•	•	•	E,•	M	•
n table.				•	•	•	•	E,•	M	•

MATERIA[…] includes integrated circuits (e.[…]

4a) Evaluation level should be used as recommendation for scope of qualification at Tier1 (given by ZVEI community).

4b) Appropriate level might varying for special cases. Please enter character accordingly.

4c) In case of different evaluation levels are affected (see 4b), the highest evaluation level will be automatically shown (in the line „Tests, which should be considered for the appropriate process change“).

Instructions how to use the DeltaQualificationMatrix (DeQuMa)
Example - DeQuMa for Active Components

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Worked on: (Name, Function)	Max Mustermann
Signature:	
Date:	
PCN number:	
For integrated circuits or discrete semiconductors select below:	AEC-Q100 Revision H

Device evaluation

MATERIAL PERFORMANCE TEST RESULTS (on the basis of AEC-Q100 Revision H)

Remarks

A letter or "•" indicates that performance of that stress test should be considered for the appropriate process change.
A @ recommended additionally by ZVEI

	CONDITIONS	No
A	Only for peripheral routing	
B	For symbol rework, new cure time, temp	
C	If bond to leadfinger	
D	Design rule change	
E	Thickness only	
F	MEMS element only	
H	Hermetic only	
J	EPROM or EEPROM	x
L	Lead free	
M	For devices requiring PTC	x
N	Passivation and gate oxide	
P	Passivation and interlevel dielectric	
Q	Wire diameter decrease	
T	Only for Solder Ball SMD	
#	Only from non-100% burned-in parts	
*	For "burn in" changes IOL or ELFR recommended	

=> Please mark 'NO' with 'x', default is 'YES'

The condition table can be found at the bottom of each matrix

5) The yellow section shows the stress tests which should be considered for the appropriate changes

6) The condition table needs to be completed for non-relevant part details
→ Please mark for ‚No' with ‚X', default is ‚YES'
(in this example J,M)

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

Example - DeQuMa for Active Components

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Hide Text

Values: Show Rows | Values: Show Columns

Form provided by ZVEI – Revision 5.0 – December 2021

Assessment of impact regarding following aspects
- contractual agreements
- technical interface of handling/processability/manufacturability of customer
- form, fit, function, quality performance, reliability

	ID	Type of change	Potential impact? No	Potential impact? Yes	Understanding of semiconductors experts	Examples to explain	Evaluation level A / B / C (A: Application level, B: Boardlevel, C: Component level, *: Not relevant for qualification matrix)	Further applicable conditions	AEC-Q100 Revision H	Check of specification (for raw material only)	Temperature Humidity Bias or biased HAST THB A2	Autoclave or Unbiased HAST AC A3	Temperature Cycling TC A4	Power Temperature Cycling PTC A5	High Temperature Storage Life HTSL A6	High Temperature Operating Life HTOL B1	Early Life Failure Rate ELFR B2	NVM Endurance, Data Retention, and Operational Life EDR B3	Wire Bond Shear WBS C1	Wire Bond Pull WBP C2	Solderability SD C3	Lead Integrity LI C6	Electromigration EM D1	Time Depending Dielectric Breakdown TDDB D2	Hot Carrier Injection HCI D3
		ANY																							
		DATA SHEET																							
		DESIGN																							
x	SEM-DE-01	Design changes in active elements. *)	P	P	Any device relevant changes in design / layout of elements with effect on specified electrical behavior. *) **Not included:** Modification to adjust product parameter within specified process window and design rules.	e.g. change of ESD structure e.g. add / remove a transistor in layout	A	Please check if data sheet is affected **(SEM-DS-01)**.	•	-	-	•	•	M	-	•	•	D,J	-	-	-	-	D	D	D
		PROCESS - WAFER PRODUCTION																							
x	SEM-PW-03	New final wafer thickness	P	P	Change in final wafer thickness.	e.g. change in final chip/die thickness	C	**A:** If thermal conductivity is affected (like MOSFET; IGBT, BGA package, stacked dies, ...) **A:** If impact on EMC or ESD behavior cannot be evaluated / excluded on component level.	•	-	-	-	E	M	-	•	•	-	E	E	-	-	-	-	-
		BARE DIE (Wafer process changes not covered in this section shall be handled according to section "PROCESS - WAFER PRODUCTION")																							
		PROCESS - ASSEMBLY																							
x	SEM-PA-05	Change of lead and heat slug plating material/plating thickness (external)	P	P	Change in material and / or process resulting in a new technology (e.g. pure tin).	e.g. change in heat slug stack e.g. change from Sn into NiPdAu e.g. change of layer thickness e.g. change of external bumps of a BGA e.g. Change of external pins of a hermetic package	B		•	•	•	•	•	M	•	-	-	-	-	C	•	•	-	-	-
		PACKING/SHIPPING																							
		EQUIPMENT																							
		TEST FLOW																							
		Q-GATE																							
		Tests, which should be considered for the appropriate process change. (7a)					A		•	•	•	•	E,•	M	•	•	•	D,J	E	C,E	•	•	D	D	D
		Tests, which should be considered for the appropriate process change after selection of condition table. (7b)							•	•	•	•	E,•	-	•	•	•	D	E	C,E	•	•	D	D	D
		Suppliers performed tests (mark with an 'X' for done or 'G' for generic)																							
		Reason for exception of tests and/or usage of generic data:																							

7a) This line provides a summary of all stress tests of selected changes excluding selection from condition table.

7b) This line provides a summary of all stress tests incl. selection from condition table* according to the recommendations of the international standards.

*(in this example J,M)

Instructions how to use the DeltaQualificationMatrix (DeQuMa)

Example - DeQuMa for Active Components

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BARE DIE (Wafer process changes not covered in this section shall be handled according to section "PROCESS - WAFER PRODUCTION")

PROCESS - ASSEMBLY

x	SEM-PA-03	Change in leadframe dimensions	P	P	Change in leadframe dimensions which has impact to the specified electrical parameter acc. data sheet or specification (e.g. heat sink, pin dimensions, die paddle size, ...) **Not included:** Variation within specification.	e. g. change in lead frame geometry	B	ESD investigations are only necessary if internal ground and power supply connection of leadframe is affected. **A:** If impact on EMC behavior cannot be evaluated / excluded on component level.
x	SEM-PA-07	Die attach material	P	P	Change of die attach material and / or process resulting in a new technology (e.g. soft solder, epoxy, etc.)		C	**A:** If impact on EMC behavior cannot be evaluated / excluded on component level (if die attach has impact on electrical conductivity).
x	SEM-PA-11	Change of mold compound / encapsulation material	P	P	Change of mold compound / encapsulation material.	e.g. change to green mold compound e.g. change of filler particles	C	**B**: impact on thermo-mechanical stress caused by mismatch of mold compound, interconnecting technology and carrier is anticipated (specific for Power Devices). **B:** for wave soldered devices **A**: in case of high frequency signals (> 3GHz) it should be assessed if possible changes in permeability of mold compound could affect signal behavior (e.g. digital signal processor).
x								...scribed under ...s applicable due to
x								...-DS-01 or SEM-DS-
x								
		Tests, which should be considered for the appropriate process change.					B	
		Tests, which should be considered for the appropriate process change after selection of condition table.						
		Suppliers performed tests (mark with an 'X' for done or 'G' for generic)						
		Reason for exception of tests and/or usage of generic data: Generic data used from one product of the product family (xxxx) which has highest performance out of that. 1 - not applicable, because SMD package; 2 - not applicable, because no change in Wafer Fab process; 3 - not applicable, for smart power devices only						

Row																										
SEM-PA-03	-	•	-	-	•	•	M	-	-	-	-	-	•	•	-	•	-	•	-	L	H	-	-	-	-	•
SEM-PA-07	-	•	•	•	•	•	M	-	•	-	-	-	-	-	-	-	•	•	-	L	H	H	H	-	•	•
SEM-PA-11	-	•	•	•	•	•	M	•	•	•	-	-	•	•	-	•	-	-	•	L	-	-	-	-	-	•
(row 4)	•	•	-	•	•	•	M	-	•	•	•	•	•	•	T	•	•	-	-	L	H	H	H	•	•	•
(row 5)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
(row 6)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	•	-	-	-	-	-	-	-	•	-
Tests, which should be considered for the appropriate process change.	•	•	•	•	•	•	M	•	•	•	•	•	•	•	T	•	•	•	•	L	H	H	H	•	•	•
Tests, which should be considered for the appropriate process change after selection of condition table.	•	•	•	•	•	•	-	•	•	•	•	•	•	•	-	•	•	•	•	L	-	-	-	•	•	•
Suppliers performed tests				G	G	G	-	G	G	G	G	G	G	X	-	1	2	X	3	G	-	-	-	G	G	G

8

9

Reason for exception of tests and/or usage of generic data:

Generic data used from one product of the product family (xxxx) which has highest performance out of that.

1 - not applicable, because SMD package;

2 - not applicable, because no change in Wafer Fab process;

3 - not applicable, for smart power devices only

8) The tests performed by the supplier should be marked with an 'X' for tests at the specific device or 'G' for generic data. For tests that were not performed, please enter a numeric value (1,2,3,..) for referencing in the explanation line (see **9)**).

9) Please provide a comment / explanation for each value (1,2,3,..) why certain listed tests are not performed or performed under different conditions.

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Example - DeQuMa for Active Components

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10) For further instructions and descriptions see sheet Guidance within the DeQuMa Excel File.

DeltaQualificationMatrix

Guidance | History | Active Components | Optoelectronic Components | MEMS | MCM | Passive Components

10